The Workings of Lightboard
Notes on the System Design and TCS Drawings

Dr. David R. Bertenshaw,　　　　Revision 1.0,　　　26th October 2020

Contents

1. <u>Introduction</u>

The Strand Lightboard (aka TCS – Total Control System) was conceived by Richard Pilbrow of Theatre Projects (TP), then theatrical consultants for the new UK National Theatre being built in the 1970s. Initial control layouts were drafted in 1973 by TP. The requirements were negotiated with Rank Strand Electric and a practical specification and contract agreed. Design commenced in 1974, with two systems installed in 1976 in the Lyttleton and Olivier Theatres. The systems continued in service until 1986, when they were replaced with Galaxy consoles. Two further systems were installed at the UK Royal Opera House and Burg Theater, Vienna.

While the system was not the first use of computers in lighting control, for example Strand had already sold many DDM systems based on a DEC minicomputer, it was ground-breaking in the scale and facilities offered. A maximum channel count of 999, up to 12 simultaneous different speed cues, recordable submasters which extended memory facilities to lighting design, integrated control of luminaire position and colour, all in a very ergonomic desk with VDUs. It provided a model for later systems to draw on; the 1980 Strand Galaxy system was a direct descendant of the system, engineered once microprocessors provided sufficient capability at low price.

However it was a very complex and hence expensive system to engineer, and in consequence found few sales. In addition, the necessary scale of the electronics led to a less than ideal reliability. A second generation system, termed TCS2, with colour monitors, floppy disc library and revised channel processing was completed in 1978, and installed in six German theatres. It remained a system for only the very ambitious (and wealthy) venues. While similar, the TCS2 design is not considered in detail here.

The functional capability of the system is well documented in commercial brochures and manuals in the Backstage Heritage Collection[1], however there is no extant documentation of the design of the system, and how the functionality was achieved. This has been achieved by scanning the old TCS/1A Maintenance handbook drawings and wiring diagrams from the Backstage Heritage collection. Although the complete handbook is absent, nearly all the indexed drawings are present and legible, with just three printed circuits and one wiring diagram missing:

6A14148	TCS OR Card, Ref 1400
6A14410	TCS A-D Card, Ref 1421
6A15777	TCS Modulation Filter Card, Ref 1454
7A14690 sht5	TCS O/S Crate Wiring Diagram.

Using this data, and various email discussions, this paper seeks to reconstruct the electronic operation of the system, from drawings and (imperfect) memory. It assumes the reader is electronically competent though not necessarily a design engineer, thus simpler functions are only summarised. It also assumes the reader has some computer knowledge. It should be read in conjunction with the Interconnection Diagram in section 20 (also available as a separate pdf file).

---

[1] http://www.theatrecrafts.com/pages/home/archive/.

These notes do not address the operational functionality, provided by the TCS User Manual and other commercial documents. They also do not consider the detail of the software in either the PDP11 or Hardware Processor, other than where it interacts with the electronics.

Many thanks are due to John Hall, Tony Brown and John Wright for their contributions.

2. **Drawings referred**

SECTION F	CARD CRATE WIRING
7A14823	TCS DESK FULL PALETTE CRATE WIRING DIAGRAM – 2 SHEETS
7A14824	TCS DESK PLAYBACK CRATE WIRING DIAGRAM – 2 SHEETS
7A19154	TCS 1A DESK PLAYBACK CRATE WIRING DIAGRAM – 2 SHEETS
8A19161	TCS 1A DESK PLAYBACK PANEL SWITCH IDENTIFICATION DRAWING
7A15344	TCS H.P. CRATE WIRING DIAGRAM – 2 SHEETS
7A14686	TCS CHANNEL O/P CRATE WIRING DIAGRAM
7A14699	TCS I/F CRATE WIRING DIAGRAM – 2 SHEETS
7A14690	TCS O/S CRATE (CORE SECTION) WIRING DIAGRAM – 5 SHEETS
7A15323	TCS TAPE CRATE WIRING DIAGRAM – 2 SHEETS
7A19162	TCS 1A TAPE CRATE WIRING DIAGRAM – 2 SHEETS
7A17830	TCS BACK-UP MASTER CRATE WIRING DIAGRAM
7A14682	TCS NON-DIM INTERFACE 80 WAY CRATE WIRING DIAGRAM
7A15676	TCS REMOTE CONTROL CRATE WIRING DIAGRAM
7A16876	TCS MODULATION CRATE WIRING DIAGRAM
7A15182	TCS STALLS CONTROL UNIT WIRING DIAGRAM
7B16539	M-BUS REPEATER BOX WIRING

SECTION H	TCS PRINTED CIRCUITS
6A14148	TCS 'OR' CARD PCB 530 REF 1400
6A14151	TCS UNIBUS TERMINATOR PCB 351/1 REF 1401
6A14154	TCS UNIBUS BUFFER CARD CIRCUIT DIAGRAM PCB 352/1 REF 1402
6A13799	TCS STATE CONTACT CARD PCB 353 REF 1403
6A14183	TCS LINE DRIVE/RECEIVE CARD CIRCUIT DIAGRAM PCB 356/4 REF 1405
6A14201	TCS LAMP DRIVE CARD PCB 362 REF 1406
6A14143	TCS INTERRUPT & DMA CONTROL CIRCUIT DIAGRAM PCB 363/2 REF 1407
6A13093	TCS UNIBUS INTERFACE CONTROL PCB 364/4 REF 1408
6A12647	TCS CHANNEL MASTER CARD CIRCUIT DIAGRAM PCB 370/2 REF 1409
6A14297	TCS CHANNEL CARD PCB 366/1 REF 1410
6A14357	TCS CORE ADDRESS REGISTER CIRCUIT DIAGRAM PCB 374/1 REF 1411
6A14363	TCS WHEEL INTERFACE PCB 376/2 REF 1412
6A14366	TCS CORE DATA REGISTER CIRCUIT DIAGRAM PCB 377/1 REF 1413
6A14390	TCS CORE CONTROL PCB 378/1 REF 1414
7A14393	TCS UNIBUS COMPUTER CONNECTOR WIRING DIAGRAM PCB 379 REF 1415 PCB 380 REF 1416
6A14398	TCS VDU REGISTER CARD PCB 381/1 REF 1417
6A14401	TCS VDU CONTROL CIRCUIT DIAGRAM PCB 382/3 REF 1418
6A14404	TCS CONTROL GENERAL CARD CIRCUIT DIAGRAM PCB 383/3 REF 1419
6A14407	TCS ALPHA KEYBOARD INTERFACE CARD PCB 384/3 REF 1420
6A14410	TCS A-D CARD PCB 385/1 REF 1421
6A14413	TCS FADE TIME CLOCK CARD CIRCUIT DIAGRAM PCB 386/3 REF 1422
6A14416	TCS WARNING CARD CIRCUIT DIAGRAM PCB 387/3 REF 1423
6C14422	TCS LOCAL TEST CARD PCB 388/1 REF 1425
6A14679	TCS NON-DIM CARD PCB 393/2 REF 1426
6A14683	TCS NON-DIM INTERFACE RELAY BUFFER CARD CIRCUIT DIAGRAM PCB 394/1 REF 1427

```
6A14687    H.P. GENERAL REGISTER PCB 395/1 REF 1428
6A14693    TCS H.P. ADDRESS SELECTOR CARD CIRCUIT DIAGRAM PCB 396/1 REF 1429
6A14696    TCS H.P. TEST & LITERAL CARD CIRCUIT DIAGRAM PCB 397/1 REF 1430
6A14765    TCS H.P. MULTIPLIER CIRCUIT DIAGRAM PCB 401/1 REF 1431
6A14768    TCS INHIBIT CARD CIRCUIT DIAGRAM PCB 402/3 REF 1432
6A14774    TCS H.P. CHANNEL OUTPUT CARD CIRCUIT DIAGRAM PCB 403/4 REF 1433
6A14831    TCS H.P. ALU REGISTER CIRCUIT DIAGRAM PCB 408/1 REF 1434
6A14777    TCS H.P. ALU CONTROL CARD PCB 404/1 REF 1435
6A14825    TCS H.P. CPU DATA GATE & STATUS CARD PCB 406/1 REF 1436
6A14945    TCS H.P. PROGRAM CARD PCB 415/1 REF 1438
6A14949    TCS H.P. CPU CONTROL CIRCUIT DIAGRAM PCB 414/2 REF 1439
6A15085    TCS H.P. EXERCISE REGISTER CIRCUIT DIAGRAM PCB 421/3 REF 144
6A14955    TCS H.P. EXERCISER CARD CIRCUIT DIAGRAM PCB 416/1 REF 1441
6A15097    TCS BACK-UP BUFFER PCB 422/1 REF 1442
6B15092    TCS 10W. AMPLIFIER CIRCUIT DIAGRAM PCB 430/2 REF 1443
6A15165    TCS TAPE WRITE REGISTER PCB 426/2 REF 1444
6A15162    TCS TAPE COMMAND REGISTER PCB 427/2 REF 1445
6A15174    TCS TAPE STATUS REGISTER CIRCUIT DIAGRAM PCB 428/2 REF 1446

6A15320    TCS TAPE READ REGISTER PCB 429/2 REF 1447
6C15335    TCS LAMP REGULATOR PCB 431 REF 1448
6C15338    PG204 POWER FAIL PROTECTION CIRCUIT DIAGRAM PCB 432
                                                   REF 1449
6A15348    TCS DATA HIGHWAY STATUS REGISTER PCB 435/2 REF 1450
6A15563    TCS DATA HIGHWAY MTX. REGISTERS CIRCUIT DIAGRAM
                                          PCB 436/1 REF 1451
6B15670    HOUSELIGHTS BUFFER CARD (NAT. & MMS) CIRCUIT DIAGRAM
                                          PCB 448  REF 1452
6A15777    TCS MODULATION FILTER CARD CIRCUIT DIAGRAM PCB 458/1
                                                   REF 1454
6B15788    M-BUS REPEATER BUFFER PCB 461/1 REF 1456
6A15774    TCS MODULATION FLASH & O/P CARD PCB 457/1 REF 1457
6C16511    MODULATION TAPE HEAD PRE-AMPS PCB 467 REF 1458
6B16709    TCS MODULATION MOTOR DRIVE & BUFFER PCB 477 REF 1459
6A16719    UNIBUS ADDRESS SWITCH CIRCUIT DIAGRAM PCB 487 REF 1460
6A16801    SPC PROM BOOTSTRAP - REF.1462
```

3. **Complexity**

The first thing that strikes one from some 45 years on, is the shear amount of electronics that was needed in the system! Some numbers:

There are 58 different printed circuit cards
There are 12 different 4U, 19 inch crates containing these cards.

The electronics total for the 620 dimmer Olivier Theatre would have been:

Racks
PDP11/35
Unibus page address switch	1 card
Ampex Core Store crate	4 x 8K18 core modules (?)
Lynwood Scientific VDU drives	3 modules
Interface crate	24 cards
Odds & Sods crate	27 cards
Hardware Processor Crate	21 cards
Channel O/P crate 1 (400 ch.)	28 cards
Channel O/P crate 2 (220 ch.)	16 cards

Non-dim Interface crate	5 cards

Desks

Desk Pallete crate	20 cards
Desk Playback crate	20 cards
Tape crate	13 cards
Remote Control crate	11 cards
Stalls Control crate	14 cards
Backup Master crate	7 cards
Modulation Trolley crate	12 cards
Total	219 cards from Strand in 13 crates.

To this more must be added from the PDP11, program and cue memory core stores and VDU drives.

PDP11/35	5 cards
PDP11 Program core	4 Cards?
Ampex Cue core store	4 Modules (2 cards each)
Lynwood Scientific VDU drives	4 Modules (2+ cards each)
M-Bus buffers	7
M-Bus PTF decoders	10 (4 cards ea?)
M-Bus 2xCC decoders	80 (3 cards ea?)
DC Power supplies	20 (Tape 2, Stalls 3, Remote 4, Modulation 3, Rack 4, Backup 2)
Grand Total	353 electronic assemblies

Since each card had 100 connections (not all used of course), and most crates had at least 12 50 way I/O connectors one can see that the connection count must have been of the order of 30,000. While all connections were gold plated, and proven reliable wire-wrap techniques were used, one should not have been too surprised at the apparent low reliability of the TCS systems. The National Theatre had also invested heavily in high technology stage machinery and flying, and consequently instituted an in-house facility for first-line electronic maintenance

4. <u>Overall Functionality</u>

The PDP11 processor communicates with its memory and peripherals via an 18 bit address and 16 bit data bus, plus control lines, termed the Unibus. The Unibus runs from the processor section to its computer memory section then out to the Strand Interface crate.

The Interface crate takes the Unibus and uses the address to route the data to whichever part of the system is being controlled. It similarly routes received data back to the processor. The presence of many sources means that a ubiquitous OR card is extensively used to combine the many incoming data streams.

All the system inputs and outputs (switches, lamps, wheels etc) each have a unique Unibus address location (i.e. are memory mapped) so the processor can directly address each component. The Unibus 16 bit data can be written/read as a 16 bit word or two separate 8 bit bytes. Most external components were byte addressed, so only 8 bit peripheral data buses were used to the remote peripherals, i.e. Desk, Stalls, Tape and Remote Control panels. Nearly all the peripherals housed in the rack with the PDP11 used the full 16 bit word.

5. __Software overview__

The system used a Digital Equipment Corporation (DEC) PDP11/35 mini-computer (see section 5 for more detail), whose program contained almost all the system's functionality. At least 8 man-years of coding went into the original software. It was designed using manual flowcharts and written in PDP11 macro assembler to enable it to run quickly enough. There is no saved record of the code structure, save it was in total some 8–90 KB in size.

The 30 ms system cycle came from some experiments, which showed that using this update period was not visible on fades and was a suitable period to scan the console buttons – you couldn't miss a button no matter how quickly it was pressed. The action processing cycle however was more relaxed, once a button was pressed you had 250 ms to show that it had been actioned (at least by toggling its illumination, preferably completion of function). If longer then the operator might press it again, thinking he had missed it in the first instance. Thus once every 30 ms cycle the fade progress was recalculated, the hardware processor re-started, the buttons scanned, and the mimics updated. Button state changes were stacked in a FIFO stack.

Interrupt requests could of course come at any time. Once out of any interrupt routine, any interrupted button processing was restarted, then newly pressed or released buttons were processed, and finally when there were no more buttons to process the VDUs were updated. Other routine background tasks included a code checksum check and the cue memory compaction/shuffle.

The PDP11 basic core program memory was supplemented by external memory, possibly from Plessey which was much cheaper than DEC memory. The 16 bit PDP11 could only address 32 Kiloword (Kw –1024 words) at a time, but more memory could be accommodated because the address bus was 18 bit. The extra address space was normally controlled by a PDP11 Memory Management Unit (MMU), however this accessory was both expensive and too complex for the task, so a Strand designed unit was used. (The DEC MMU was used in the TCS2.)

The PDP11 memory space was split into 8, 4 Kw pages. The bottom 6 pages were used for permanently resident code and working data areas, while the 7th page was used for paged code, which included all of the button action code and display code. The top (8th) page was always mapped to I/O address space including access to the cue core store. Calls from one paged section of code to another was handled by using the emulator trap (EMT) in resident code, which stacked and switched page registers appropriately.

The cue memories were held in a separate core store array made by Ampex. It was logically organised as a memory heap. Cues were compacted and thus variable in length dependent on the number of circuits in use, so when a cue was updated the new copy was put on the top

and the old copy flagged as deleted. A background memory shuffle periodically scanned cue memory and shuffled cues up to recover space from deleted cues (akin to modern disc defragmentation). A separate index was needed, partly because the cue could be anywhere in the core and partly because of the cue numbering scheme (non-contiguous and with decimal cues). The linkage records of where the cues were located remained in the PDP11 data memory, thus particular care had to be taken when servicing to not overwrite these, else the cue memories were lost. Loading the standard lighting program and service program tapes preserved this data.

The main program could be boot loaded from tape and started from the console. A hardware test program was also provided to test the peripherals, which could also be boot loaded from the console. The program tested all peripherals for correct functionality, needing operator interaction to test the desk functions. Full details are provided in the "Hardware Test Program – Operating Instructions" document in the same folder as this file.

A set of magnetic tape utilities were provided to generate program and post-mortem tapes, to duplicate tapes and to use a paper tape reader. Full details are in "T.C.S Magnetic Tape Utilities" document in the same folder as this file.

6. **The Digital Equipment Corporation PDP11/35**

There is an interesting back story to DEC and the PDPs. In 1957, Ken Olsen and Harlan Anderson founded Digital Equipment Corporation (DEC), initially selling digital industrial logic systems with some limited programmability. They wanted to call their company Digital Computer Corporation, but their venture capitalist investors insisted that they avoid the term Computer and hold off building computers. It was then 'widely known' that proper 'Computers' required large computer centres with many staff, and furthermore, there was only a world need for some 100 systems! So by using the term 'Programmable Data Processor', or PDP, DEC avoided this stereotype. Further their systems were much cheaper ($100K vs $1M), could be bought rather than leased, and easily adapted by the user. By 1960, it had become clear that their smaller machines were real computers (then termed mini-computers), but the PDP brand was now established. A wide range of machines was introduced in the 1960-70s varying from 12–36 bit size. However Ken Olsen was also not an infallible prophet, having pronounced in 1977 'There is no reason anyone would want a computer in their home.' (He clarified it later as meaning home automation.)

The PDP11 was DEC's range of 16 bit mini-computers. The first was the PDP11/20, followed by the second generation PDP11/40, the PDP11/35 being its OEM version. It was leading edge for the time, the range only having been introduced in 1970, with a list cost around US$20K. At that time this was comparable to the average price of a London house (£10K). Strand had already chosen to use the earlier PDP11/15 (OEM version of the 11/20) in DDM for the Royal Shakespeare Theatre at Stratford, installed in 1971. Consequently there was experience of using and interfacing to this range of machines.

When TCS design commenced, the first and only microprocessor that existed was the Intel 4004, derived from a desk calculator. It had just 4 bits and instructions took 10–20 μs to execute, vs the PDP11 which executed 16 bit instructions in 1–4 μs. The largest scale integrated circuits were 1024 bit MOS memory chips. However digital logic integrated

circuits, esp. the ubiquitous and fast TTL system introduced in 1966, were now well established. This made TTL the natural choice for the various computer interface systems.

Strand also had the existing DDM system to build on. The method of interfacing to the PDP11 was known, with long distance interfaces to console buttons and mimic designed and shown to be reliable. However the complexity demanded by the new specification required a much larger scale of interfacing, together with designing solutions to the new video interfaces, remote controls, a tape system and especially the challenge of processing up to 999 channels in up to 63 fades.

7. <u>The Unibus and its Address Space</u>

The Unibus is the PDP11 computer data bus used to communicate between the processor and its program and data memory and any peripheral interfaces. It is physically a flat cable of 56 signals and 64 ground lines, and daisy-chains between the system units. It is resistively terminated at each end, with one end usually the processor, the other the last peripheral interface. In TCS the Unibus runs from processor to extended memory chassis to the Interface Crate.

The PDP11/35 is a 16 bit CPU with 18 bit physical address. However A0 (lowest address bit) is an upper/lower byte address, so for 16 bit data words it has a 128 Kiloword (Kw) address space. However its PC and other address registers are only 16 bit, the peripherals are assigned a 4 Kw region, so the concurrent code must reside within 28 Kw. In consequence the extra address space is normally paged and mapped to allow program expansion. In TCS Strand designed its own memory page switch card (a simple MMU) to fit in the CPU which used a Zone Address register. (TCS2 used the standard DEC KT11-D MMU.) The PDP11 instruction set permits writing position independent code, however the paged code was compiled to execute in its expected locations.

DEC uses the octal system for binary notation, where each group of 3 bits is numbered 0–7. Consequently the 16 bit program addressable space has a maximum of 177777, while the whole 18 bit address space extends to 777777. The address space is conventionally divided into program and data space, extended program space and peripheral address space. Since both program and data are held in read/write core store, there is no hardware distinction between program and data, it is left to the software to organize any boundaries. Since the sole program running is the lighting software, no distinction or protection is made between operating system and functional code.

The PDP11 system uses memory mapped peripherals, where all external interfaces occupy addresses within the normal address range. By convention, all peripheral addresses are logically in the range 160000–177777, i.e. the top of the normal addressable range. However, hardware in the processor automatically translates this range to 760000–777777 on the Unibus. The system address map is shown below.

Address range	Function
000000 000777	Program area for start-up vectors, interrupt vectors, traps etc.
001000 137777	General program to 24 Kw
140000 157777	Extended program page of 4 Kw Mapped by Zone Address (ZA) to [ZA]0000 to [ZA+1]7777 Only active if ZA>0.
160000 177777	Peripheral address space. Program access to this space is automatically converted to 760000–777777
200000 757777	Extended program area of 23 x 4 Kw pages. Each page mapped by Zone Address to 140000–157777
760000 777777	Peripheral address area of 4 Kw All peripherals can be read and/or written to, and sectioned as below.
763776	Extended address Zone Address register.
764000 765777	Peripheral region M0 Desk panels
766000 766177	Peripheral region M8 Stalls panel
766200 766377	Peripheral region M9 Interrupt timer, Fade time clock and rack contacts/mimics/temp. sensors
766400 766577	Peripheral region M10 Tape interface
766600 766777	Peripheral region M11 Remote Control panel
767000 767177	Peripheral region M12 Video drives
767200 767377	Peripheral region M13 Not used
767400 767576	Peripheral region M14 Cue Core Store and Data Highway (MBus)
767600 767776	Peripheral region M15 Hardware Processor
770000 777777	Reserved for DEC peripherals and processor addresses. System printer used standard DEC peripheral interface (probably DL11)

The detail of the addresses used and the purposes of each bit are documented in the TCS1/1A FLM, Appendix C, Hardware Address Maps, which should be found in the related document cache to this file.

Curiously for very little saving in logic, the peripheral address regions M0–15 were not fully decoded, with A13–16 ignored. It was assumed the processor was addressing this region if solely A17 was set, thus preventing any extended address core exceeding 32 KW. This did not become a problem.

The Unibus permits interface devices to take control of the bus to directly read or write data to core via Direct Memory Access (DMA). The Hardware Processor used this to read each

channel's current Stage levels, with the recomputed Stage level then written back the original location. This occured for all channels once per cycle (approx. 30 ms).

Devices can also interrupt the PDP11 to demand a rapid programmatic response. Four Unibus interrupt levels are provided, BR4–7. The interrupt passes an interrupt vector byte on the bus containing the program location to jump to, to service the interrupt. In most cases a status bit is also set in the interface's register to signal the precise function requiring service.

Interrupt	Vector	Source
BR4	274	Data Highway, ready to send
BR5	174	VDU Control, ready to write
BR6	270	Hardware Processor, cycle complete
BR7	170	Tape Read/Write buffer and Fade/Real Time clock.

The system printer used a standard printer, the DECwriterII (LA36 introduced 1974). This supported 30 cps printing and also a current loop interface, necessary for the long run from racks to control room.

The Unibus is an active low, open-collector, 5 V bus with dedicated DEC driver and receiver chips. The basic operation is asynchronous. The bus master (usually the PDP11) asserts the address, and the data lines if writing. An Msync signal is then asserted to trigger a read or write at the peripheral, which when complete, and the data lines have been set for read, a corresponding Ssync signal is sent back by the peripheral. This then completes the cycle, the processor cancels Msync which cancels Ssync. This permits slower peripherals, esp. those very distant such as Lightboard's desks, to readily interact as normal. However the PDP11 Msync signal has a 15 µs time-out to protect against mal-functioning peripherals, which had to be specially extended at the National Theatre to ~25 µs to accommodate the very long cables to the desk and stalls. (This non-standard modification always caused problems for visiting DEC engineers!)

8. The Consoles

The consoles carried the operating panels and displays with their interface electronics in the plinth. The interface to the computer rack was via parallel address and data buses, using high speed, differential line driver/receivers.

Figure 1. National Theatre, London

Figure 2. Royal Opera House, London

9. The Main Racks

Unfortunately, no images can be found of these, apart from the layout drawings in the TCS2 user manual shown below. Two 19 inch racks were needed to house the PDP11, cue core store, hardware processor, video drives, interface electronics and power supplies.
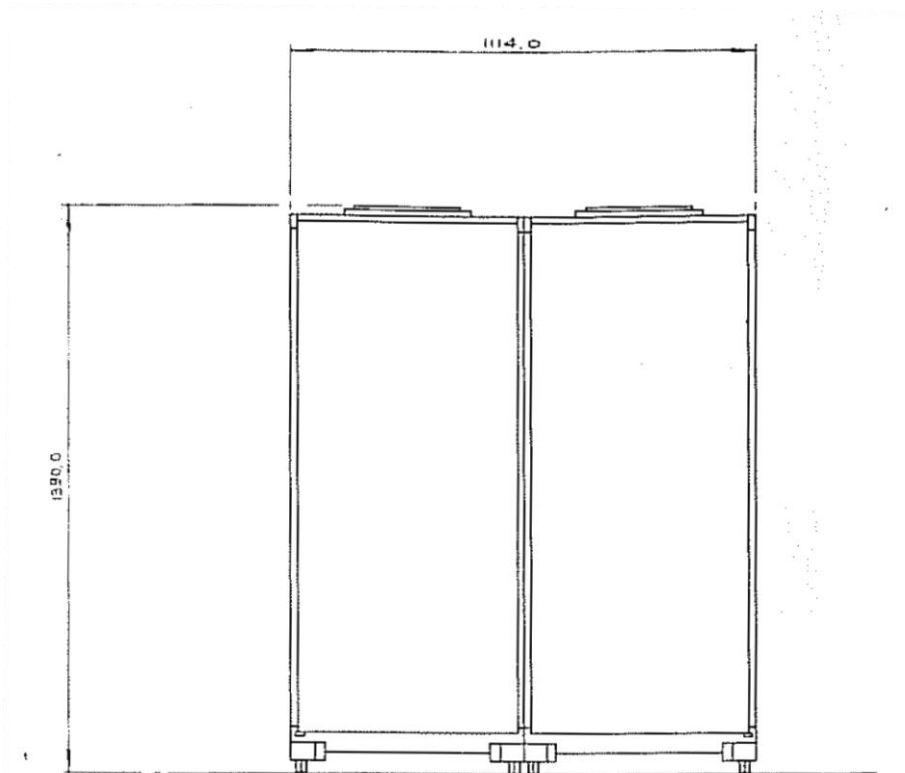

Figure 3. TCS2 system racks

10.   The Interface Crate

This received the Unibus and terminated it. The address lines were buffered for distribution to the various peripherals. The data lines were buffered twice, once for 16 bit peripherals, and again for 8 bit peripherals. All remote desk peripherals, the VDU and DP & LC used 8 bit data, the other rack interfaces used 16 bit data.

The OR cards (containing 8 channels of 8-input OR gates with dual outputs) served both to buffer data and address lines and to collate incoming data from up to 9 sources.

The Unibus addresses dedicated to the various hardware elements are decoded in the dedicated user address space. The 1 Kw space 764000–767777 is decoded by the Interface Control into 9 segments, a 512 word space (M0) used for the main desk, and 8 other smaller 64 word spaces used for other areas (M8–15). The decoding is done by developing dedicated Msync signals for each segment (Mx), so that that segment then only needs to consider the lower order address signals A0–9. The Ssync response from each segment is selected dependent on the Msync asserted.

The buffered 10 bit Address and 16 bit Data lines with control signals are output at TTL level to the two local crates, Hardware Processor and O&S (Core). Similar lines but with 8 bit data are output to O&S Crate for the VDUs, Fade time clock and local contacts.

For the remote consoles, four bidirectional balanced line systems support the Desk, Stalls, Tape and Remote Control panels. These used SN75107 & SN75110 chips, driving twisted pair cables with 110 Ω termination each end, developing approx. -600 mV differential signals. This system supported a -3/+5 V common mode range. For each remote console connection, a balanced power fail signal was also fitted, shorted by an active console. Thus if the console was unpowered or unplugged, this inhibited the line receivers to prevent noise detection. A telephone wire pair with jack socket outlet was connected in common to all four remote consoles to support a maintenance intercom.

Two interrupt control cards, each servicing two interrupts, generate the Unibus interrupt routine in response to interrupt request signals from Tape, Data Highway, VDU, Hardware Processor and Fade Time Clock.

11.   The Hardware Processor (HP)

This hardware processed the actual channel levels. While the PDP11/35 could perform a hardware multiply, it was not fast enough for 999 channels and the computer was anyway very busy with the massive supervisory task needed to interact with two operators and three VDUs.

Each channel could be processed on any fade controller. These controllers could be channel controls, palette masters or playback fade controllers (up and down separately). Consequently there were 64 controllers, 63 active ones and a null controller. Each controller could also operate in Group or Cue mode. Since each channel could only be on one Fade Controller at a time (thanks to latest-takes-precedence operation), the computation (Group or Cue) was only done once per channel.

In Group mode, all channels changed by the same amount as the fade controller, and channels which reached full or zero before the others would still respect their offset if brought back to the start. The extra under/overflow value for channels that had reached full or zero prematurely was stored in the Stage store lower byte. The fade controller could only span -100% to +100%, thus the under/overflow value never exceeded 377.

The classic digital cue fade algorithm is Signal_out = Fade_progress*(New_preset - Old_preset) + Old_preset. This was simplified by making New_preset - Old_preset = Channel_Increment, and the HP only being provided with the change in Fade_progress that cycle (Fade_Increment). This made the cyclic cue computation:
New Stage_Value = Old Stage_value + Fade_Increment*Channel_Increment.

Consequently in Cue mode the channel changes by the amount of the fade controller (Fade_Progress) change multiplied by the Channel Inc. The Channel Inc. is computed by the PDP11 once as the difference between the stage level and the intended new cue at the start of the fade. The fade controller can only span 0% to +100%, however the cyclic Fade Inc values can be positive for a progressing cue or negative for a cue being reversed.

The Fade Inc change values were thus 'drip-fed' in real time by the PDP11 as the fades progressed. By this means the operator/PDP11 could speed up, slow down or even reverse the stepping of the internal value for "Fade_Progress" and the fade for that channel would faithfully follow. There was no general or FOH master, these were always done with cues. The Fade controller could be set to BO, Flash Full or Flash out all its the channels, processed also by the HP.

The target for the HP was to process 999 channels in <30 ms, so had to complete in less than 30 us per channel. The solution was to design a special stored program processor solely to perform this, with the code in two 256*4 bit Schottky fuseable link PROMs to give 256*8 bit instructions. The instruction clock rate was 6.14 MHz giving an instruction cycle time of 163 ns. This was >10x the speed of the PDP11, albeit implementing a much simpler instruction set. The 31 instructions were always two 4 bit values, 15 instructions which carried an associated 4 bit parameter, the 16th encoding 16 direct instructions. They all executed in one cycle except Branch where the Goto address was in the following 8 bits and Set Literal where the 16 bit value was set in four such instructions. There were also conditional branch to subroutine tests (on true or false) which also saved the program counter (PC) value to allow a return from branch.

The PDP11 could write to all the HP registers and take over program execution for testing purpose, plus there was a physical test card with indications and single-step control.

There were seven, 16 bit General Registers carrying the various fade and computation parameters, plus five dedicated registers. They were:
- S0, Channel Inc Address.
- S1, Stage Store Address.
- S2, Fade Processor base Address (offset by Channel Inc Fade Processor no.).
- S3, Channel Inc value inc. Fade Processor no.
- S4, Stage Store value.
- S5, Fade Inc change in that cycle.
- S6, Channel Output pre curve lookup and BO/Flash controls.
- S7, Channel Output post curve lookup and BO/Flash controls.
- S10, Channel No.
- S14, Hardware multiplier, hard-wired to bits 0-7 of S3 and S5.
- S16, Literal register.
- S17, ALU register.

Its numeric heart elements were a 16 bit ALU (Arithmetic Logic Unit to add/subtract/shift/rotate), a Test and Literal control, and an 8*8 = 16 bit hardware multiplier. An internal 16 bit data bus connected the selected general registers to the ALU system to compute the levels. Data was passed from register to register with two instructions, DATOC output a named register on the internal bus, DATIC then input the data on the bus to another named register.

The actual HP program is not listed, but the essential procedure is believed to be as below.

1. PDP11 computes for a Cue the Channel Inc value for every channel, sets the relevant Fade Processor in the Channel Inc lower bytes, and clears the Stage Store lower byte.
2. PDP11 writes maximum channel number to S10, and DMA addresses to S0, S1 and S2.
3. PDP11 sets Interrupt enable and starts HP.

   HP now runs independently of PDP11.
4. HP starts 30 ms Cycle timer.
5. DMA input channel data into S3 and S4 using S0 and S1 addresses
6. DMA input Fade processor data into S5 using S2 offset by the S3 Fade processor No.
7. Test S5 (Fade Inc) bits 0-7 (the fade controller no.). If = 000 (no fade) Goto step 11.
8. Test S5 (Fade Inc) to determine if a Group or Cue fade
9. For a Cue fade
   a. S14 triggered to multiply bits 0-7 of S5 with bits 0-7 of S3, giving 16 bit result.
   b. S4 loaded to ALU.
   c. Test S5 for fade direction (bit 8?).
   d. Test S3 polarity for up/down (bit?).
   e. S14 multiply result added or subtracted to ALU.
   f. ALU result bits 0-15 loaded back in S4.
10. Else, for a Move fade
   a. S4 loaded to ALU.
   b. Test S5 for fade direction (bit 8?).
   c. Add or subtract S5 bits 0-7 to ALU bits 8-15. Leave ALU bits 0-7 unaltered.
   d. If ALU overflows, set ALU bits 8-15 = 377 and add S5 bits 0-7 to ALU lower byte.
   e. If ALU underflows, set ALU bits 8-15 = 000 and subtract S5 bits 0-7 from ALU lower byte.
   f. ALU result bits 0-15 loaded back in S4.
11. S5 bits 9-14 set BO, DBO, Flash Full/Out in S7 in hardware.
12. Test previous demultiplex channel output strobe complete, else wait until complete.
13. ALU bits 8-15 loaded to S6.
    This triggers a 25 μs demultiplex strobe to the demultiplex channel output crates.
14. DMA output Stage level from S4 using S1 address.
15. Test S10. If >0 signals more channels to process.
   a. Decrement S0, S1 & S10.
   b. Goto step 5.
16. Else test cycle timer expired. If false, wait until expired.
17. Set BR4 Interrupt and wait for restart.

The Multiplier card used a shift-add method to multiply 8*8 bits into a 16 bit accumulator. It took 9 cycles of the program clock, giving a result in ~1.5 μs. This did not delay the program, as other operations could continue simultaneously.

The Data Gate card receives and latches the data from the PDP11 to present to the recipient register, or sends the selected register data to the PDP11. It also holds 4 bits of status information, as given below.

Bit	Status Function
0	NPREN, testable by Program card, permits program run.
4	SPR, spare
5	CPINH, Inhibits channel outputs (prevents flicker during testing)
6	INTEN, Interrupt enable.

The CPU Control card interfaces the HP to the PDP11, decoding the address. To simplify individual selection of the several identical cards, the 8 bit address region is decoded into 16 X and 16 Y selection lines, with the each addressed card connected to the appropriate X/Y pair. The sectioned MSync signal M15 actions a read or write, with the X and Y signals combining address selection and strobe. The card also interfaces the DMA and Interrupt signals to the Interface crate, and contains power failure detection circuits.

The Address Selector card selects the required S0/1/2 address for DMA cycles.

Four OR cards provide data collection and interface buffering.

The Exercise Card allows the PDP11 to stop/continue execution, reset the program address and to load an instruction for execution. It can also read the program address.

The HP card crate required over 30 amps @ 5V!

12.   Channel Output Crate

The HP outputted the stage level (8 bit) and channel number (10 bit) directly in digital form to separate crates of 400 channel output D/A demultiplexer cards. A Channel Master card receives the digital signals and an 8 bit D/A converter converts the level to 0 to -10 V analogue. Two analogue multiplex signals are output for odd and even channels in the sample and hold cards, since the 25 µs demultiplex strobe was too short to reliably analogue sample with economic components. Thus an odd and even demultiplex strobe samples the relevant analogue streams in the 16 way Channel cards.

The Channel cards used bipolar 741 opamps with FET sample gates. The opamps have a deliberate positive bias to offset the opamp's input current, to minimise per-cycle drift. Further to protect the stage lighting in case of cessation of HP or PDP11 operation, a 5 second time-out sensed lack of data, and then activated a 5 sec further delay then a forced 10 second fade to off for all channels.

This was well known to National Theatre operators. If the system hard warning sounded continuously, indicating a computer crash, they had just 10 seconds to sort out a backup state via the pin-patch before the stage started a relentless fade to zero!

A dimmer inhibit signal could be wired into the dimmer outputs via diode gating to reduce overall levels in case of a supply overload.

13.   The O&S Crate – Core section

The cue storage used up to 4 Ampex core store modules of 8K18 format. The extra two data bits supported parity systems, not used on TCS. The total was thus 32 Kw. The cue memory was compacted to only record active channels, and consequently cue files were variable in size.

The core address was formed in a Core Address Register card, which held a 16 bit core word address (A0-15). This could be written and read by the PDP11, hence the cue core data presented as a single word address. After each read or write it auto-incremented by one. Thus, while the PDP11 could not easily randomly address the core, it could very easily stream sequential data.

The 4 core addresses were formed from a X/Y matrix decode from A0-6. The sectioned MSync signal M14, if A5=1, actioned a read or write, with the X and Y signals combining address selection and strobe. A power supply sensing system detected out-of-spec supplies with ac fail sensor also inhibited the core stores.

14.   The O&S Crate – Data Highway section

This section drives the M-Bus data highway used to control the remote control luminaires (pan/tilt/focus), colour and slide changers. It shares data distribution logic with the Core Store section.

The M-Bus was a balanced 2-wire and ground synchronous signaling system. The data consists of a 40 bit packet, with 0101 preamble, 32 bits of data and a 4 bit CRC checksum. Position data was resolved to 1 in 1000. Line idle was logic 1. The data was phase encoded and transmitted at 48 Kbaud, with a >100 μs frame gap. It was implemented as unidirectional but provision was made for a return signal. The phase encoding ensured the data was self-clocking on reception.

The true and false MTX signals switch between 0 to -5 V on a twisted pair bus with rise and fall times of 1 μs and with 100 Ω termination. True signal MTX is -5 V for logic 1. The repeaters and receivers were specified to accept a +/-100 V common mode range, so the bus could tolerate fierce interference.

The interface to the PDP11 was handled by the generic Control General card. This also responded to Msync M14, if A5=0, for read and write, and interfaces address lines A0-7 to decode to a 16x16 X/Y matrix for byte addressing, with the X and Y signals combining address selection and strobe.

The Data Highway was controlled by two cards, the Status Register and MTX Data Register. The MTX Data Register received two words of data into a shift register, this was topped and tailed with the preamble and checksum, then phase encoded during transmission. The packet was automatically transmitted after loading the second data word. On end of transmission a ready signal (TXRDY) was set.

The Status register signaled an interrupt on TX ready. Several read-only bits signaled error states and if TXRDY was true. Write-only bits enabled the TXRDY interrupt.

15.   The O&S Crate – Video section

The console displays were monochrome CCT monitors. These were driven by bought-in video drives from Lynwood Scientific Developments Ltd. There was provision for up to 4 displays, but only a maximum of 3 were used. These drives only updated data during the video flyback periods, so could only be written to intermittently, when they declared they were ready. The display was 80x30 character display of upper case and numeric only (apparently 7x5 pixels per character).

The interface to the PDP11 is handled by the generic Control General card. This responds to Msync M12 for read and write, and interfaces address lines A0-7 to decode to a 16x16 X/Y matrix for byte addressing, with the X and Y signals combining address selection and strobe.

The VDU Control card holds a 4 bit status register and an 8 bit data buffer for video byte data. Of the status register bits, 4 can be written to reverse drives 1/2 and 3/4 and one to reset the video drive power fail status bit. Four are readable but only two were used, D7 = video drive ready, D4 = video drive power OK. The data buffer assumes ASCII character coding, and intercepts codes 140-177 (octal) to perform video control actions. These codes are not passed to the video drives, but select which of the 4 drives to write to and enable/disable cursors. The card also receives the selected drive ready signal, triggering an Interrupt and setting the Interrupt status bit.

The dual VDU Registers interface the character data to the actual video drives. The character data is latched ready for the drive, and when the selected drive goes ready, signaled by the interrupt, character data is written until the ready status goes false again. Controls select the cursor to be off/blinking/on. It is assumed that cursor positioning within the drives used ASCII control characters.

16.   The O&S Crate – Local Contacts and Mimics section

The O&S crate also monitored local temperatures, provided a Fade Time clock and 8 local test switches and lamps. The interface to the PDP11 is handled by the generic Control General card. This responds to Msync M9 for read and write, and interfaces address lines A0-6 to decode to a 16x16 X/Y matrix for byte addressing, with the X and Y signals combining address selection and strobe. An OR card collects the multiple read data inputs.

The Fade Time clock divides a 12.288 MHz crystal to provide a 204.8 kHz clock and a 2048 Hz clock. The first clocks a 256 divider, preset by the PDP11, providing a timed interrupt after loading from 4 μs to 1.25 ms later. The second slower clock also drives an 8 bit counter up to 255, signaling periods up to 125 ms, and is cleared whenever read. Thus this signals in each cycle (typically 30 ms) the elapsed time of that cycle to permit accurate cumulative fade times.

A Contact card and Lamp drive card drive 8 switches and lamps on a plug-in card, and connect to internal rack signals. It is not clear what these are, but probably included local overtemperature sensors.

17.   The Desk, Stalls and Remote Control Crates

These provide the interface to the console controls, detecting button presses and wheel movement, and illuminating button mimics. The balanced address and data transmission lines from the Interface crate are received on identical Line Drive/Receive cards, with OR cards used to buffer and distribute mimic data and collect contact data. The Desk used two crates, one to interface all the playback controls, and a second for the palette controls. The Stalls and Remote Control crates were designed in a common format to the Desk, differing only in the lower quantity of contacts, mimic and wheels. They all contained local Warning cards.

The interface to the PDP11 was handled by the generic Control General card. This responded to Msync M0 for read and write, and interfaces address lines A0-9 to decode to a 16x16 X/Y matrix for byte addressing, with the X and Y signals combining address selection and strobe. Even though the maximum 1024 byte address space exceeded the X/Y decoding capacity, in practice the total quantity used was less than 256 bytes, so only a single matrix was required.

Push buttons were read by the State Contact cards. These read the state of 24 grounding button contacts (0 V = true) in 3 addressed bytes. Each button had a 10 ms time constant buffer for noise and contact bounce rejection. The alphanumeric keyboard had a dedicated Alpha Keyboard Interface card. The parallel interface from the keyboard strobed each character into a buffer, which the PDP11 could read. A second read address was used to clear the buffer ready for the next character, which could not be input until either the existing character had been read or cleared.

The desk mimics (nearly all button illuminations) similarly supported 3 addressed bytes of open-collector lamp drives, capable of driving 12 V/100 mA or 5 V/200 mA lamps. A diode gated lamp test signal was provided but apparently not used.

The desk wheels were required to provide a full fade of 256 steps for a single human sweep of the exposed wheel. The exposed wheel quadrant was about 90° and probably 250 count/rev industrial encoders were used. These were two-phase incremental encoders requiring 5 V lamp drive and outputting differential signals. These provided four edge changes per step, detected in the dual Wheel Interface card. The up/down changes incremented/decremented (2's complement) an 8 bit counter cyclically read then cleared by the PDP11, to accumulate the next cycle. Logic prevented the counts exceeding 1xx upwards or 2xx downwards, no matter how fast the operator moved the wheel.

The Desk crate also contained the System Warning card. This contained two tone generators, a Soft warning one at 190 Hz and a Hard one at 700 Hz, both pulse modulated at 2 Hz. These also drove warning lamps as well as an audio output (not known where this signal went, but it was reportedly clearly audible). The Warning card had a single byte address that could be written to sound either warning, and a timer that if it was not re-started at least every 250 ms, would automatically sound the hard warning. This indicated a processor failure/crash. The Warning card also contained a 900 Hz stepped wave tone generator and an up to 177 programmable divider providing a monophonic tone source. Two switchable filters, a 120 Hz low-pass and a 1500 Hz hi-pass and a 3 step attenuator completed a rudimentary musical ability. However it is believed this was only ever used at a Strand party!

The Modulation Trolley input was analogue. This was interfaced by up to 3 two channel A-D cards, whose details are missing. The common intercom telephone signal terminated in a jack socket on the rear panel.

18.   **The Tape Crate**

This provided the interface to the tape control panel and the tape transport, used for both cue library storage and program loading. The crate detects button presses and switch states, illuminates button mimics, controls the tape transport and reads and writes tape data. The system used the Quarter Inch Cassette (QIC) two track system with DC 300 cartridge. The Tape drive was the PG-204 by Penny & Giles (probably a variant of the PG-200).

Figure 4. DC300 Cartridge

The balanced transmission lines from the Interface crate are received on identical Line Drive/Receive cards, with OR cards used to buffer and distribute data. Buttons and switches are read by State Contact cards and mimics driven by Lamp Drive cards identically to the Desk crates, with the interface to the PDP11 similarly handled by the generic Control General card on interface M10.

The desk-mounted tape drive was a self-contained unit with its own power supplies, motor drive electronics and tape head read and write amplifiers. It received a set of TTL level signals to operate it. These could command it to load a tape (rewind to beginning), run forward/backward, select Track 1 or 2, and search forward/backward (for next data block or End of File). For reading and writing, the drive received a write enable and write data, it signaled if write protect was set on the cassette, and output a read enable signal, read data and a recovered read clock.

Data was written phase-encoded at 48 kb/s, in 10 bit characters of 8 data bits, a stop bit and odd parity bit, taking 208 μs in total. The characters were written in packets with a 0101010101 preamble, data bytes as required, then a null last character with the stop bit set followed by the same preamble again as postamble. The postamble ensured that a valid data block could be recognised regardless of the tape motion direction. The End of File (EOF) was signaled by absence of data for >188 ms. There was no facility to overwrite records other than a complete erase, all new data was appended.

The Tape drive was controlled and interfaced by four dedicated cards, the Tape Command Register, Tape Status Register, Tape Read Register and Tape Write Register. The Tape Command card can be written by the PDP11 with a 4 bit operational Command Code (details below) and Interrupt enable (bit 6). This is converted into a sequence of low level commands by a stored program in a 1702 EPROM, which steps though up to 16 states. There were no conditionality tests (as in the HP), however each step could be paused while the step completed, or the sequence aborted in case of error. Timed waits of 43–680 ms could be

commanded, to enable pre-determined gaps to be written.

Command Codes	Function
0	Do Not Use
1	Start Read
2	Start Write
3	Write Continuous File Gap
4	Stop
5	Space Reverse Block
6	Write Block Gap
7	Write File Gap
8	Find Load Point – Track 1
9	Unload
10	Go to Beginning of File
11	Go to End of File
12	Find Load Point – Track 2
13	Space Forward Block
14	n/u
15	n/u

The Status Register allowed the PDP11 to read a byte of status bits (listed below). The read Parity Request indicated a read parity or preamble error. Status bits shown * caused an Interrupt (BR7) if set.

Status bit	Function
0*	File Gap Found
1	Tape Safe (file protect tab set)
2*	Abort (excessive servicing delay or data already present when reading started)
3	Load Point found
4*	Not Busy
5	Power Off or Cassette Out
6*	Parity Request (read and write)
7*	Data Request (read and write)

The Write Register contained a 12.288 MHz clock, divided down to 96 kHz for program control and 48 kHz for data clocking. A byte of data could be written by the PDP11, which was serialized, parity generated and phase encoded for the Tape drive. An error was flagged if the next byte was not serviced in time. At start of writing, the first byte was automatically the preamble. The write Parity Request came from the Read Parity error, indicating that the system had the ability to read data as it was being written (i.e. two heads).

The Read Register received the data from the Tape Drive, with data and clock already recovered. A Data Present signal from the drive was used to enable reading and to enable searching for data gaps on the tape, with a 188 ms gap needed to signal File Gap Found. The received data was converted to a byte for reading, except for the first byte which was tested for correct preamble code. An error in pre-amble or parity flagged a read Parity Request. If the data buffer was not read in time before the next byte, the Abort error was set.

21

A separate lamp supply to the mimics was regulated off the main +5 V supply by a Lamp Regulator card with separate intensity control to the main desk.

A system failing was that the magnetic tape could get corrupted by power cycles, so cassettes had to be removed before any power up/down. This led to the problem that the loading of a new PDP11 program after a crash required an operator at the desk to load the cassette, and an operator at the PDP11 to start the boot program. Savy solo engineers solved this by manually entering a short program that simply looped on testing a desk button, then when at the desk, the engineer pressed the button and the program jumped to the boot code. This was solved in TCS2 by a remote boot facility.

The common rack/desk intercom signal terminated in telephone jack sockets on the crate rear and front panels.

19.   The Modulation Trolley

The Modulation Trolley was a system to provide the Pallete masters with an external modulation source for flashing effects or a variety of sound-to-light modulation for subtle or pre-recorded changes. It has 4 identical channels for the 4 Pallete masters. It was separate to the main TCS system and portable and could be plugged in as desired. External audio inputs or two internal compact cassette tape drives allowed pre-recorded sound to be used for the modulation.
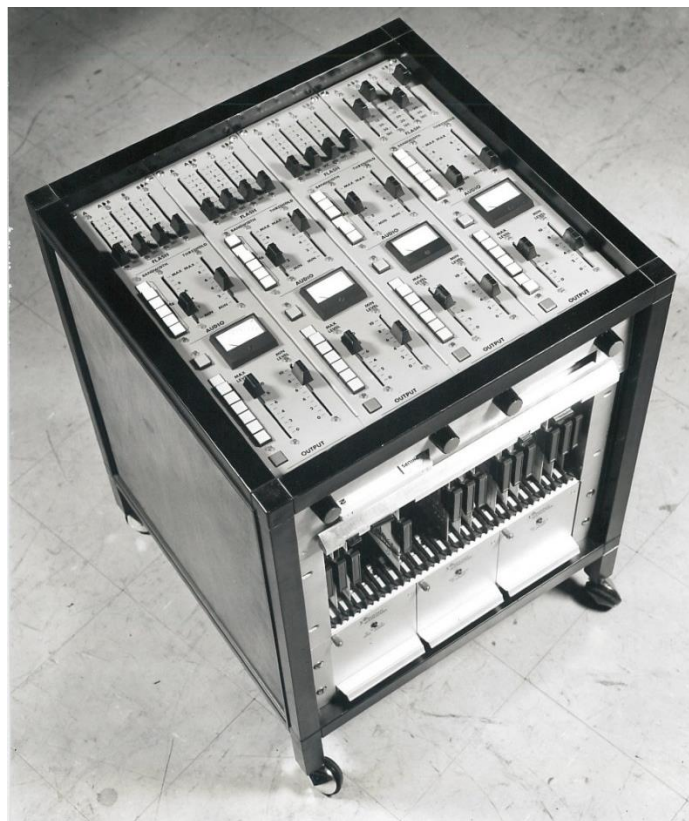
Figure 5. TCS Modulation Trolley

The Flash and Output card provided a 4 phase flash sequence, with controllable rise, on, fall and off times of 0.1–30 s, plus controllable off and on levels. This used a voltage controlled oscillator to drive an 8 bit up/down counter, with the output via a D/A converter. There was no sequencing between the channels.

The Modulation Filter card (circuit missing) provided a range of frequency filters, plus a variable control for the bandwidth of the filter and the amplitude threshold for detection.

The internal source for each submaster could be selected with controls for maximum and minimum. An internal amplifier and monitor loudspeaker provided for sound identification.

20. Lightboard, TCS Interconnection Diagram

Rack

Desks

Rack section:

Unibus

Unibus Terminator

Program Core store

Strand Unibus Address Switch and Terminator

DEC Processor

PDP11/35 Cabinet

Unibus Buffer (Address)

Unibus Buffer (16 bit data)

Unibus Buffer (8 bit data)

Interupt Control x2

Interface Control

M0-15
S0-15

Interrupts x4

OR Card (D0-7 out)

OR Card (D0-7 in)

OR Card (Address)

OR Card x2 (D0-15 in)

OR Card x2 (D0-15 out)

OR Card x2 (D0-7 in/out)

Line Drive/Receive x2 (D0-7, A0-9) — Desk

Line Drive/Receive x2 (D0-7, A0-9) — Stalls

Line Drive/Receive x2 (D0-7, A0-9) — Tape

Line Drive/Receive x2 (D0-7, A0-9) — Remote Control

Interface Crate

M14

Core Control — Core Address — Core Stores x4

OR Card x2 (D0-15 out) — Core Data

O&S Crate (Core Section)

M14

Control General — Data Highway Status

Data Highway Data Register — M-Bus

O&S Crate (Data Highway)

M12

Control General — VDU Control — Video Drives x4

VDU Register x2

O&S Crate (Video Section)

M9

Control General

OR Card

Lamp Drive — Local Test Card

Contacts

Fade Time Clock

O&S Crate (Local Contacts and Mimics)

Hardware Processor Crate:

CPU Control — M15

Data Gate and Status

OR Card x2 (D0-15 in)

OR Card x2 (D0-15 out)

Address Selector (DMA)

Exercise Register (or manual Exerciser)

Program

Processor bus

General Register (GR) x3

GR Fade Proc+ Channel Inc

GR Fade Inc

GR Circuit No

ALU Control

Multiplier

ALU Register

Test and Literal

GR Stage Store

Channel Output

Hardware Processor Crate

Start Channel Card No.

Channel Master

Channel Card (16 ch) x24 — 400 Dimmers

Overload Inhibit — Current sensors

Channel Output Crates

Desks section:

Interface Crate M0/8/11

Line Drive/Receive x2 (D0-7, A0-9)

Control General

OR Cards

Lamp Drive — Desk mimics

State Contacts — Desk Buttons

Wheel Interfaces — Wheels

System Warning

A/D

Alpha-Kb Interface — Alpha-Keyboard (desk)

Desk/Stalls/Remote Control

Modulation Filter — Frequency Controls

Modulation Flash & O/P — Flash Controls

Amplifier

Modulation Motor drive

Modulation Tape Pre-amp — Cassette Tape Transports

Modulation Trolley

Interface Crate M10

Line Drive/Receive x2 (D0-7, A0-9)

Control General

OR Cards

Lamp Drive — Desk mimics

State Contacts — Desk Buttons

Tape Command Register

Tape Status Register — Power Fail

Tape Read Register — Tape Transport

Tape Write Register

Tape

Lightboard, TCS Interconnection Diagram
Rev 1.0
David Bertenshaw, 29-sept-2020