

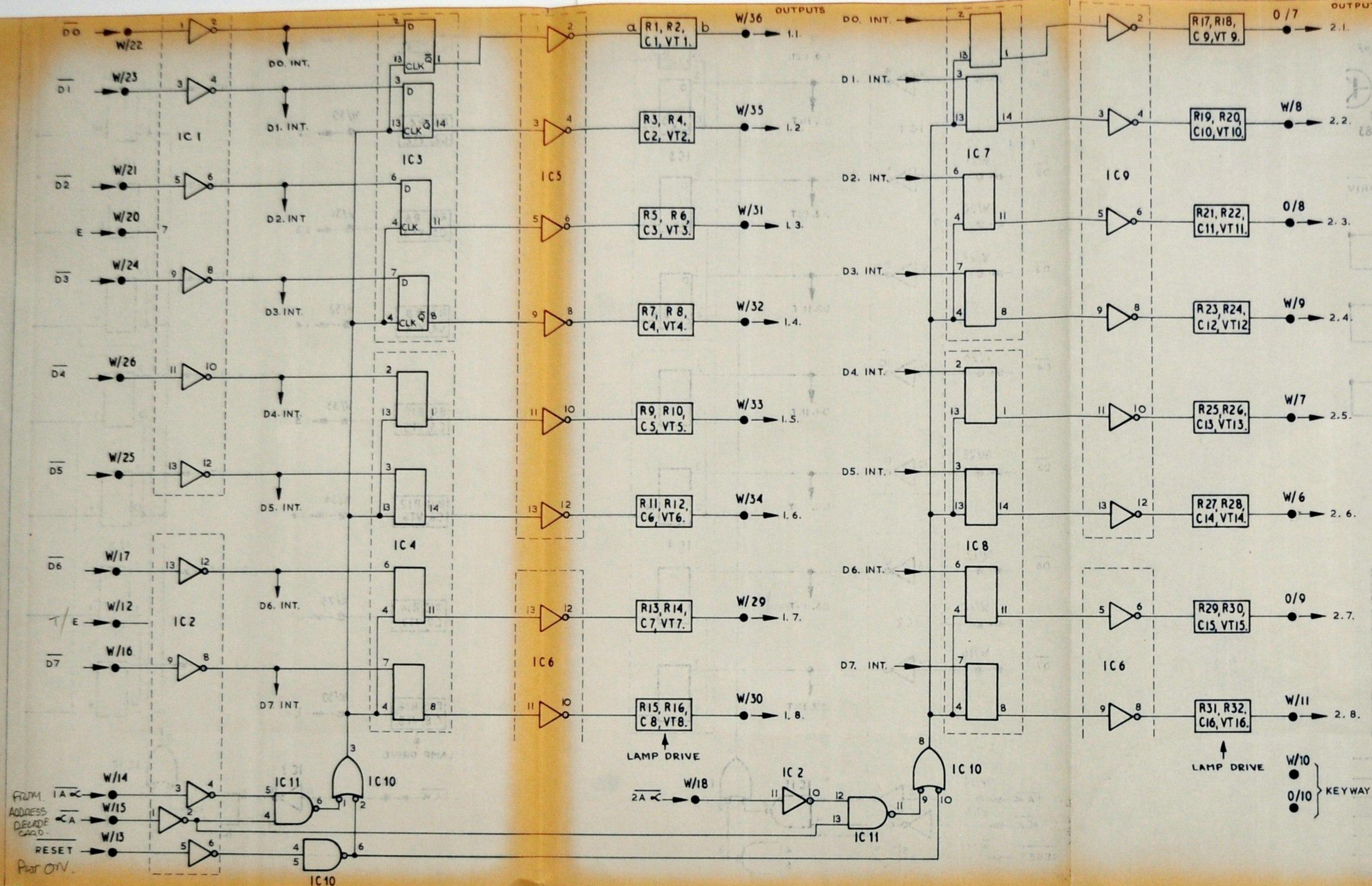


D.D.M. 2

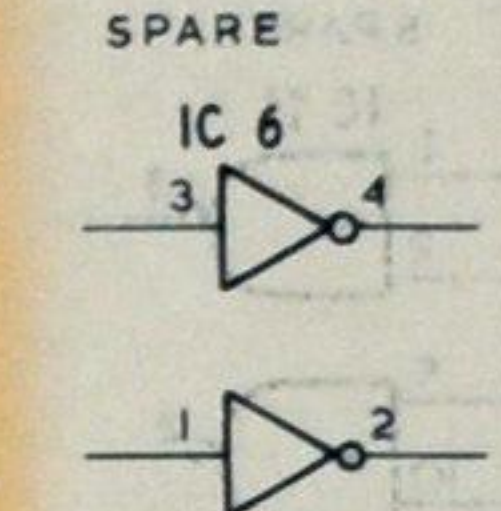
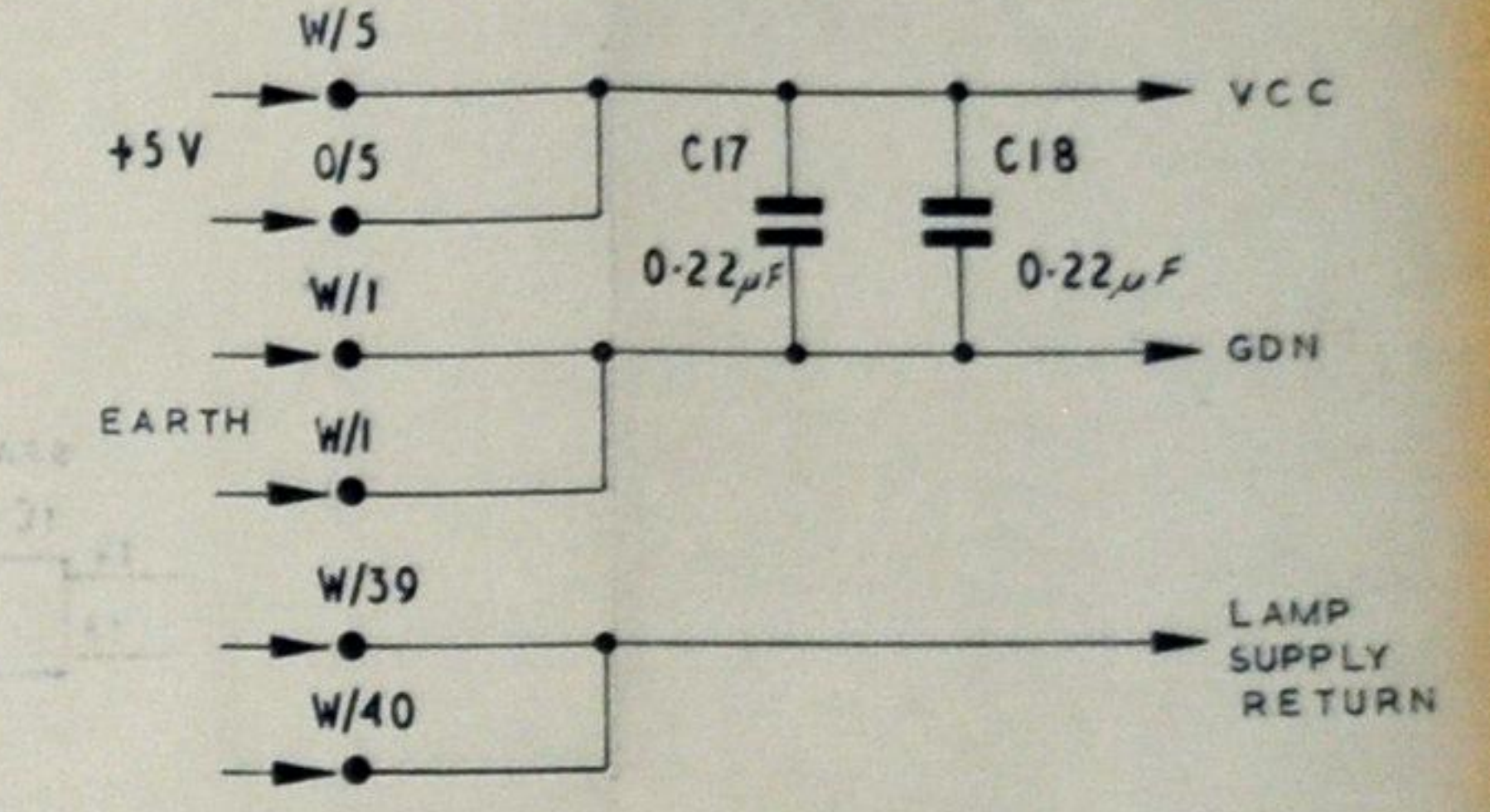
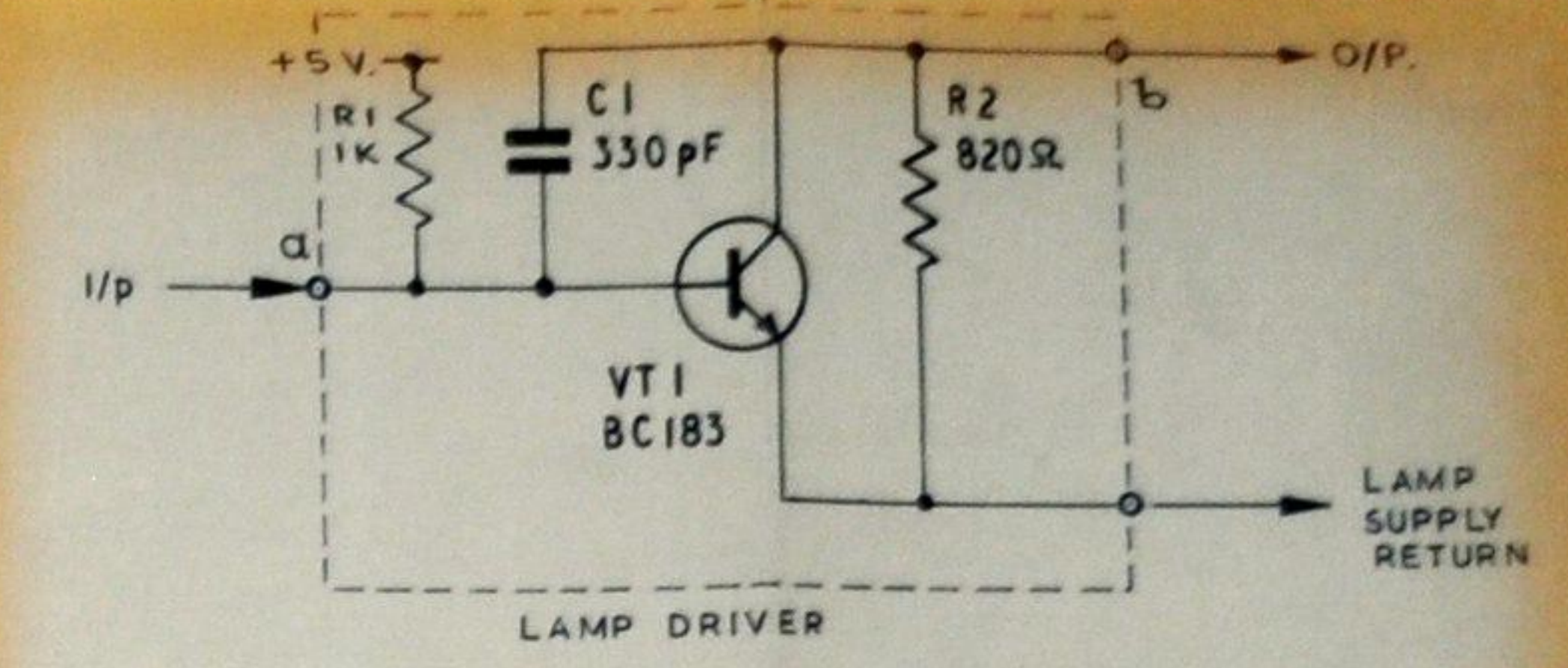
DRAWING SET

D.D.M.2

DRAWING SET



INTEGRATED CIRCUITS			
REF. No	TYPE	+VCC	GDN.
IC1, 2.	SN74LO4N	PIN 14	PIN 7
IC3, 4, 7, 8.	SN74L75N	" 5	" 12
IC5, 6, 9.	SN7405N	" 14	" 7
IC10.	SN7400N	" 14	" 7
IC11.	SN74LOON	" 14	" 7



ALL RESISTORS ARE 1/4W, 5%
UNLESS OTHERWISE STATED

P.C.B. DRG 5B01250

SCHEDULE 5501281

ISSUE	DATE	SIGNATURE
B	11-10-72	
A	6-12-71	

TITLE

D. D. M. 2.

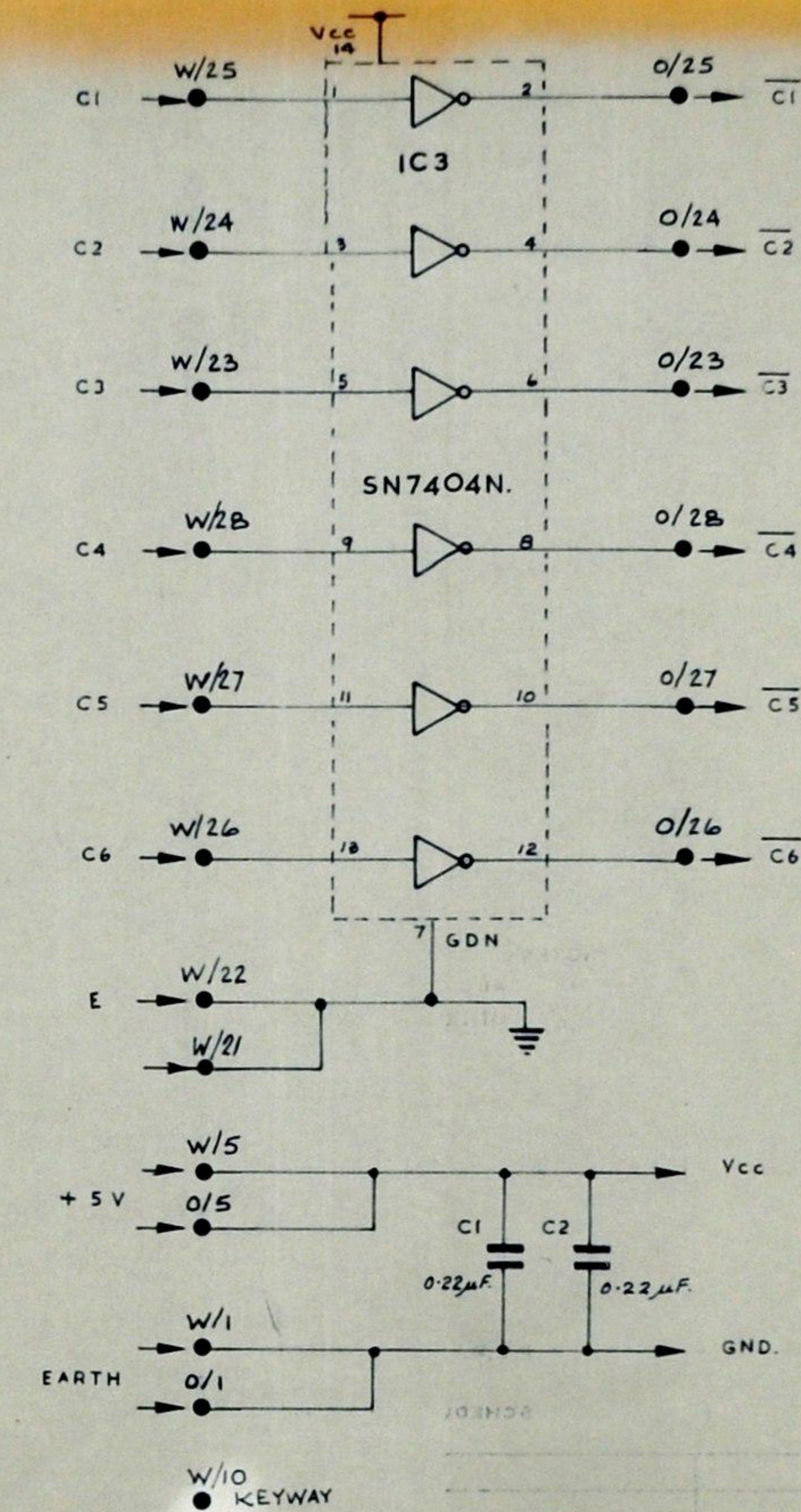
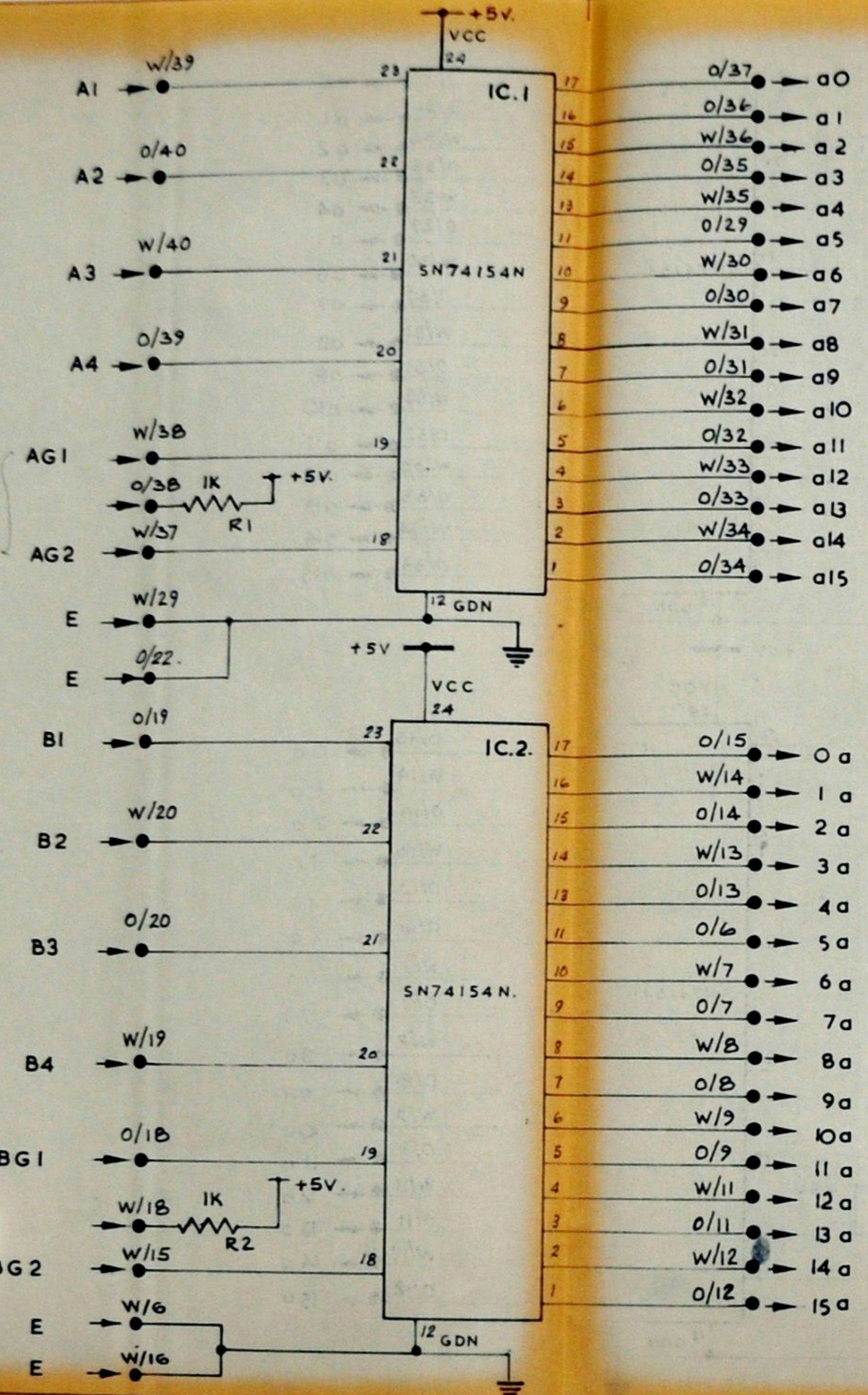
16 BIT STORE & LAMP
DRIVE LOGIC DIAGRAM

REF. 1200 PCB 211

DRG. No 6B01200

High active
used to .25

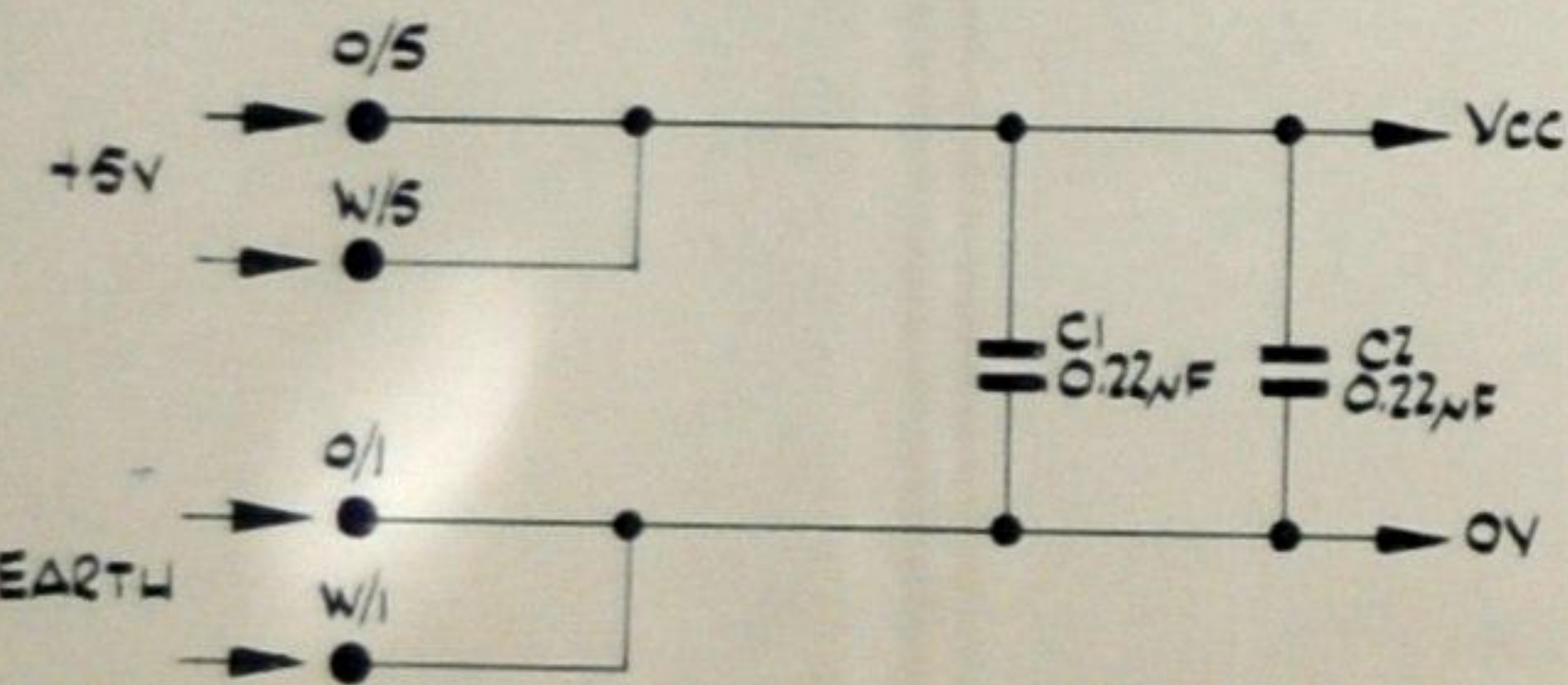
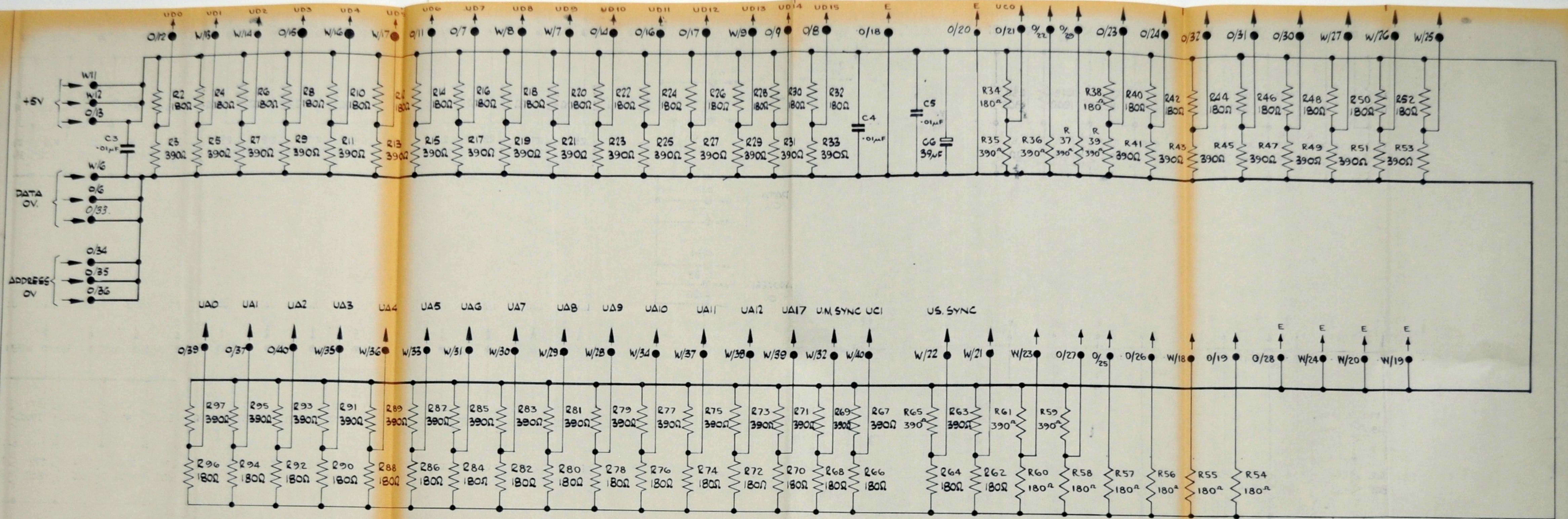
High active
used together
to stroke



NOTES:
ALL RESISTORS ARE 1/4 W UNLESS OTHERWISE STATED

P.C.B. ORG. 5801262
SCHEDULE 5501237

			TITLE	D. D. M. 2
			ADDRESS DECODE LOGIC	
			DIAGRAM.	REF 1201
			PCB 212	
B	11 12 72	R. Eason		
ISSUE	DATE	SIGNATURE		
			Drg.No.	6801201



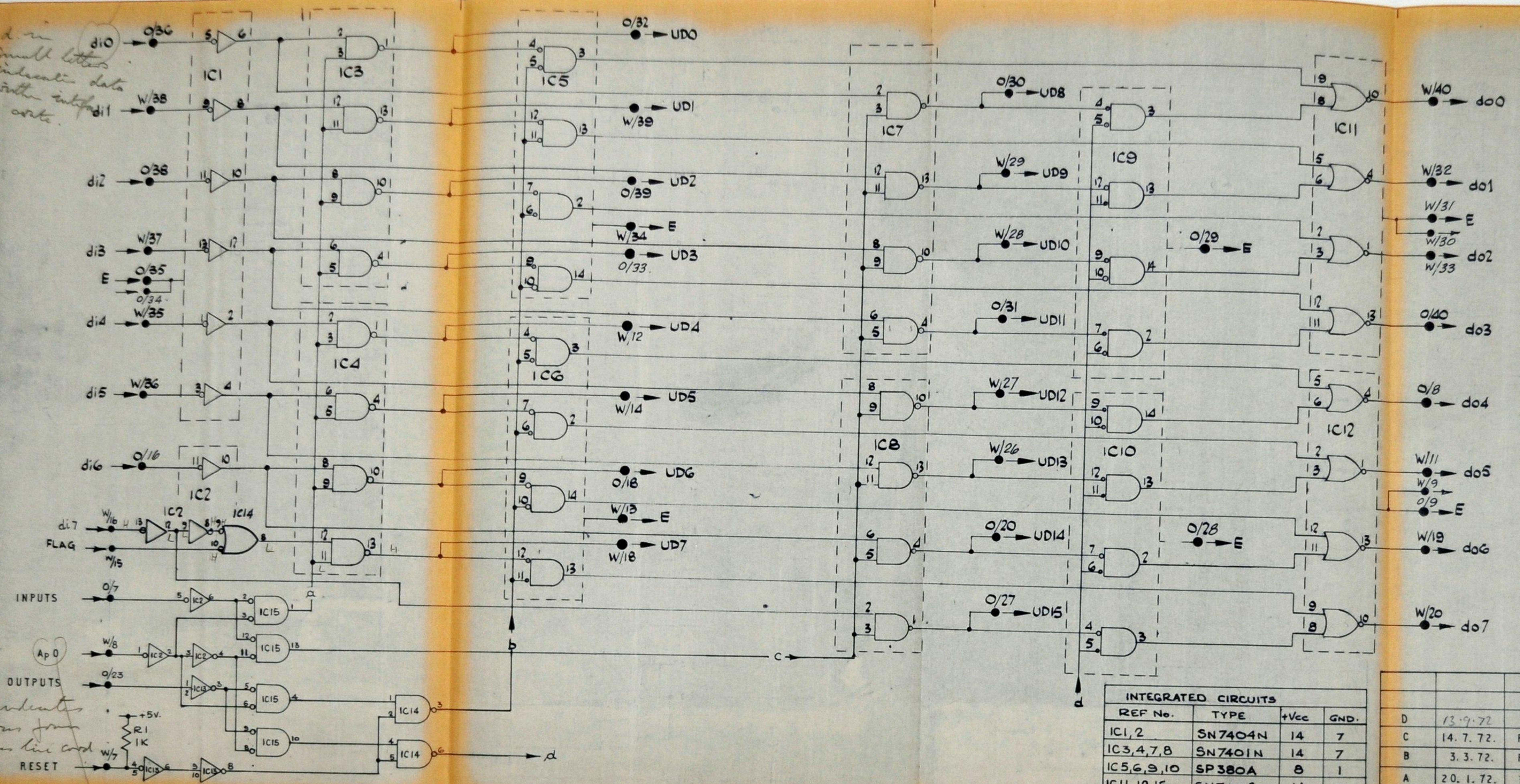
O/10
W/10
KEYWAY

NOTE :-
ALL RESISTORS ARE 1/4W 5%
UNLESS OTHERWISE STATED.

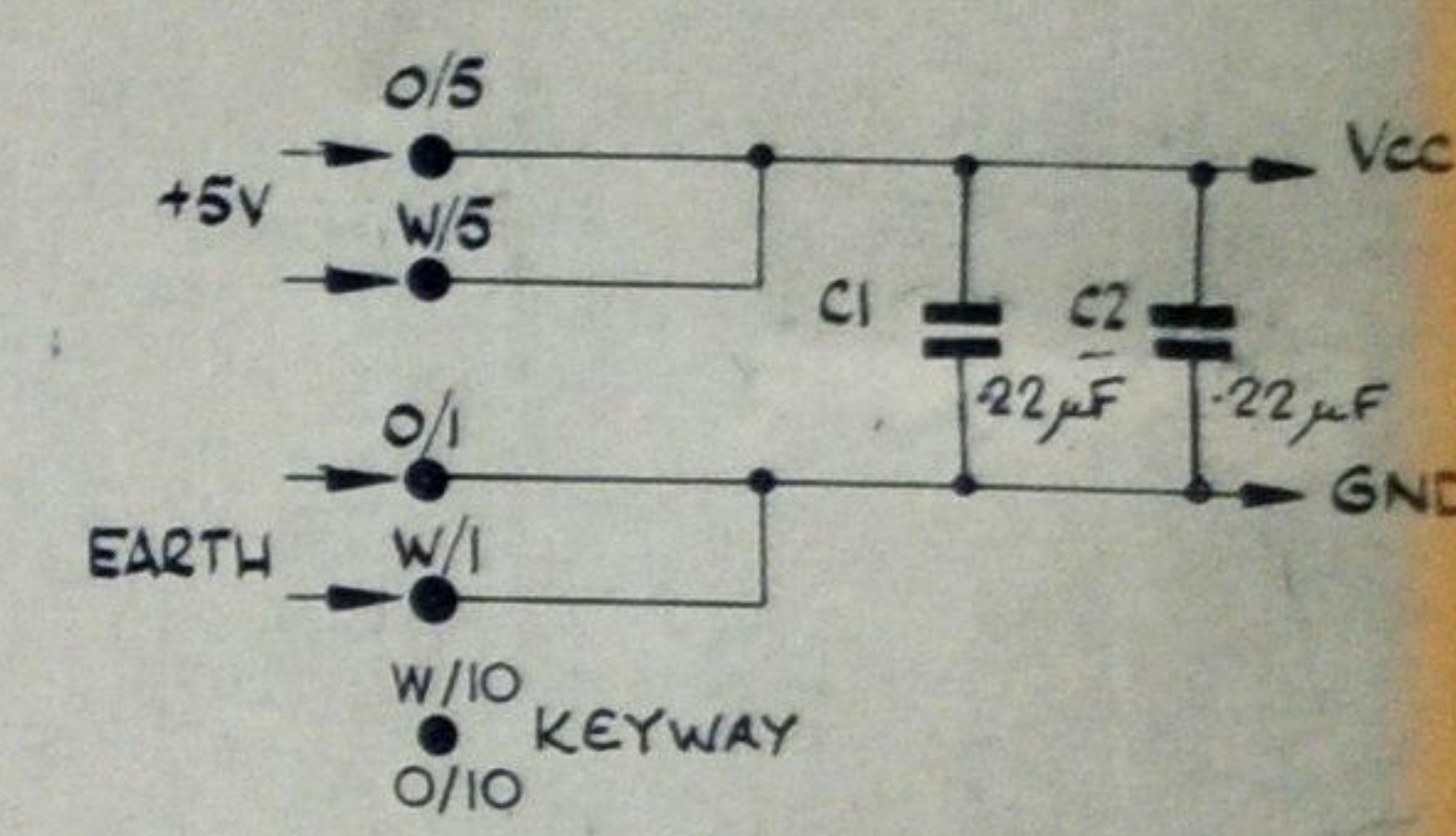
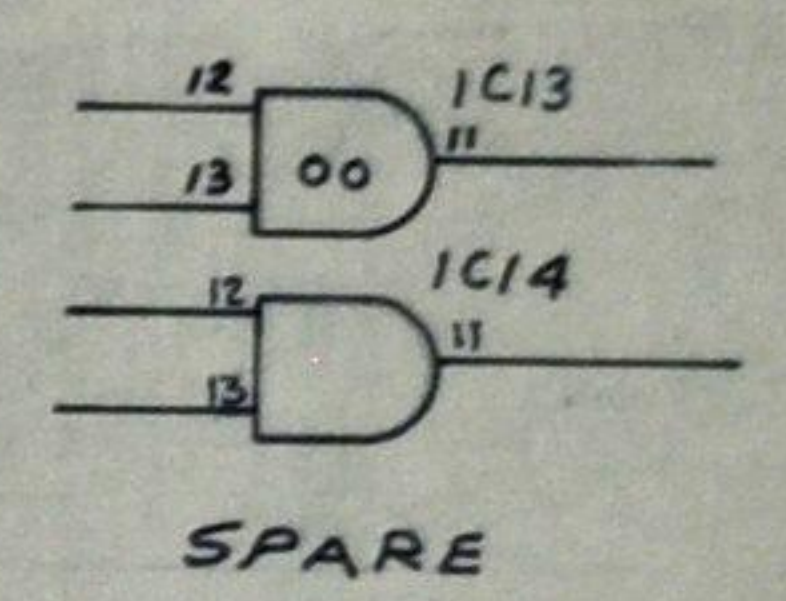
P.C.B. 5301251
SCHEDULE N° 5501290

TITLE:-		
Pdp.11 UNIBUS TERMINATOR		
PC.213/1 REF 1202		
C	5.10.71	R.12
B	22.7.71	R.12
A	20.1.72	R.12
ISSUE	DATE	SIGNATURE
DWG N° G801202		

Small letters
indicate data
within interface
code.



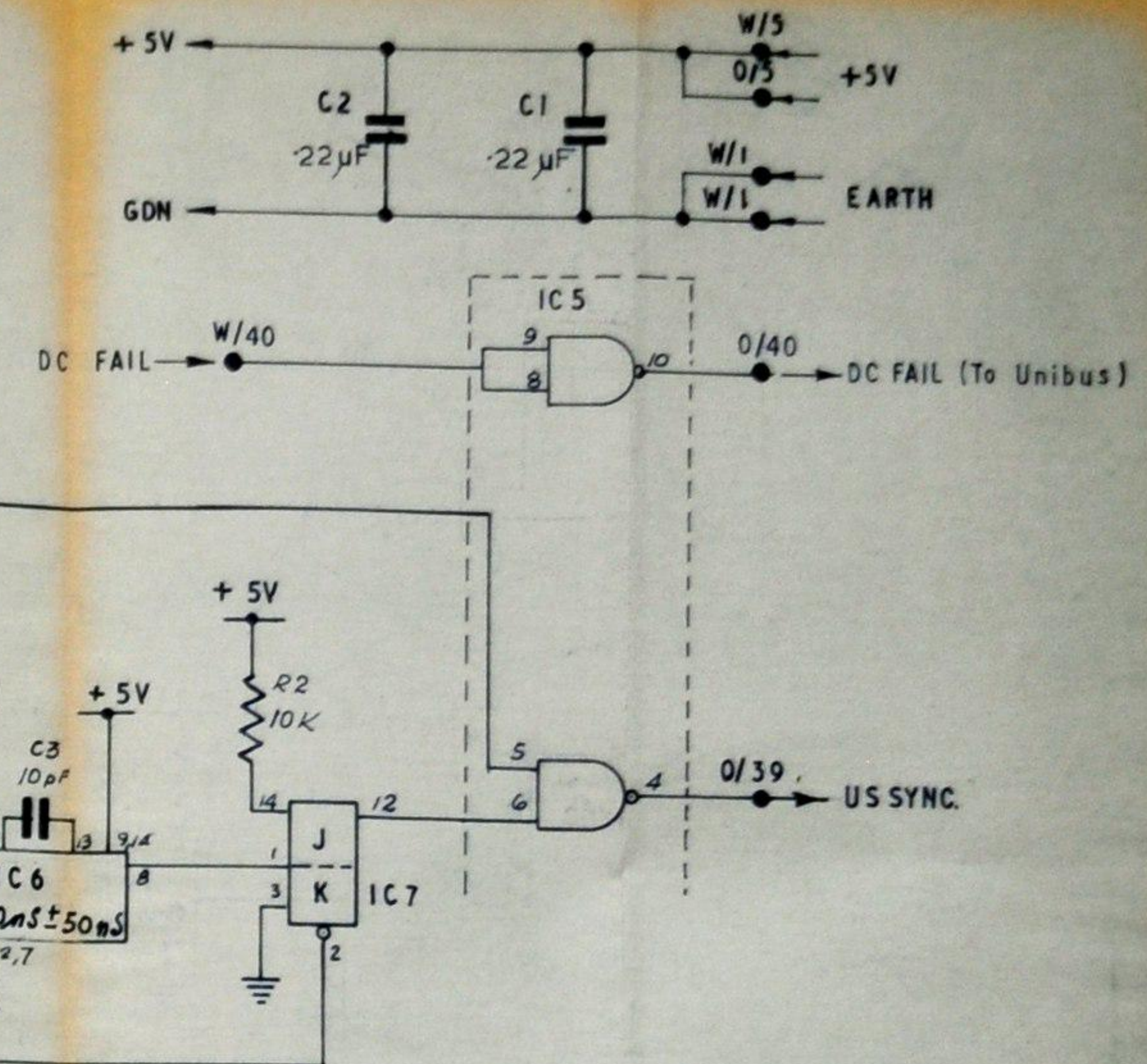
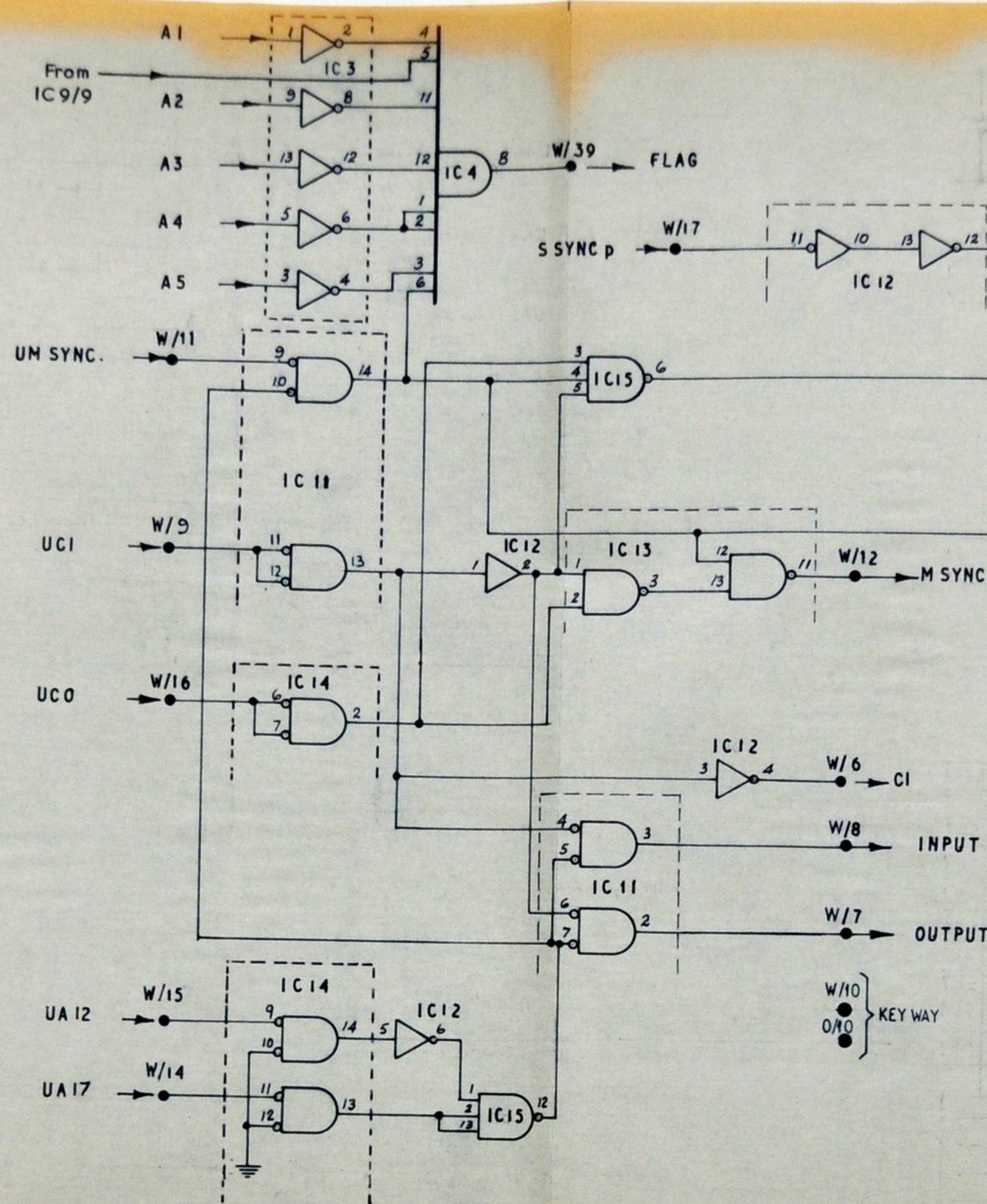
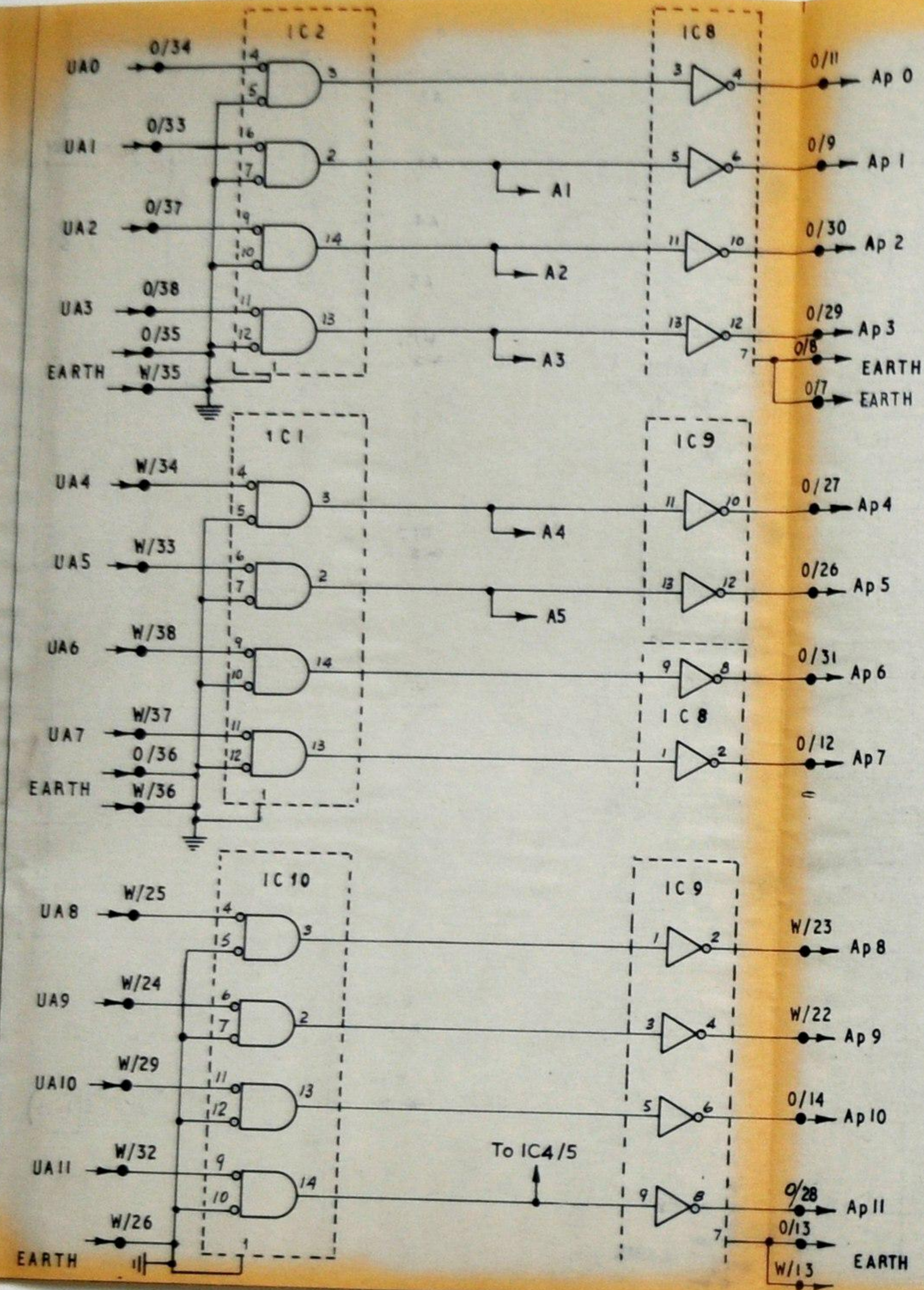
Printed
address from
allow line code
RESET



P.C.B. DRG. 5B01252
SCHEDULE 5S01284

INTEGRATED CIRCUITS			
REF No.	TYPE	+Vcc	GND.
IC1,2	SN7404N	14	7
IC3,4,7,8	SN7401N	14	7
IC5,6,9,10	SP380A	8	1
IC11,12,15	SN7402N	14	7
IC13,14	SN7400N	14	7

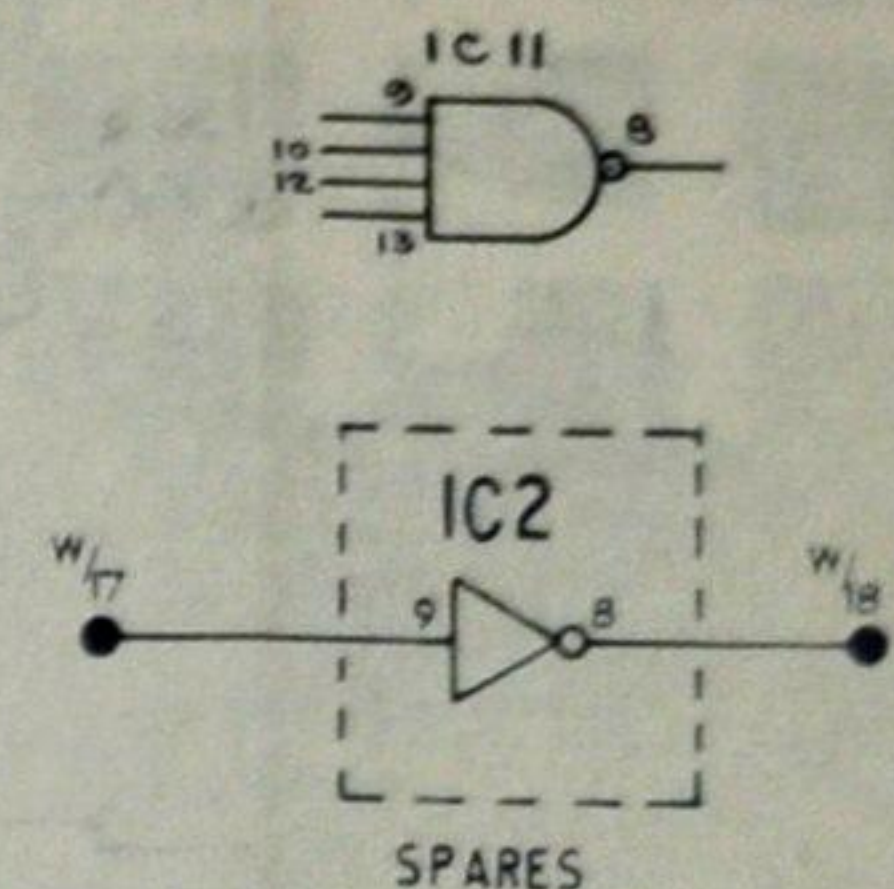
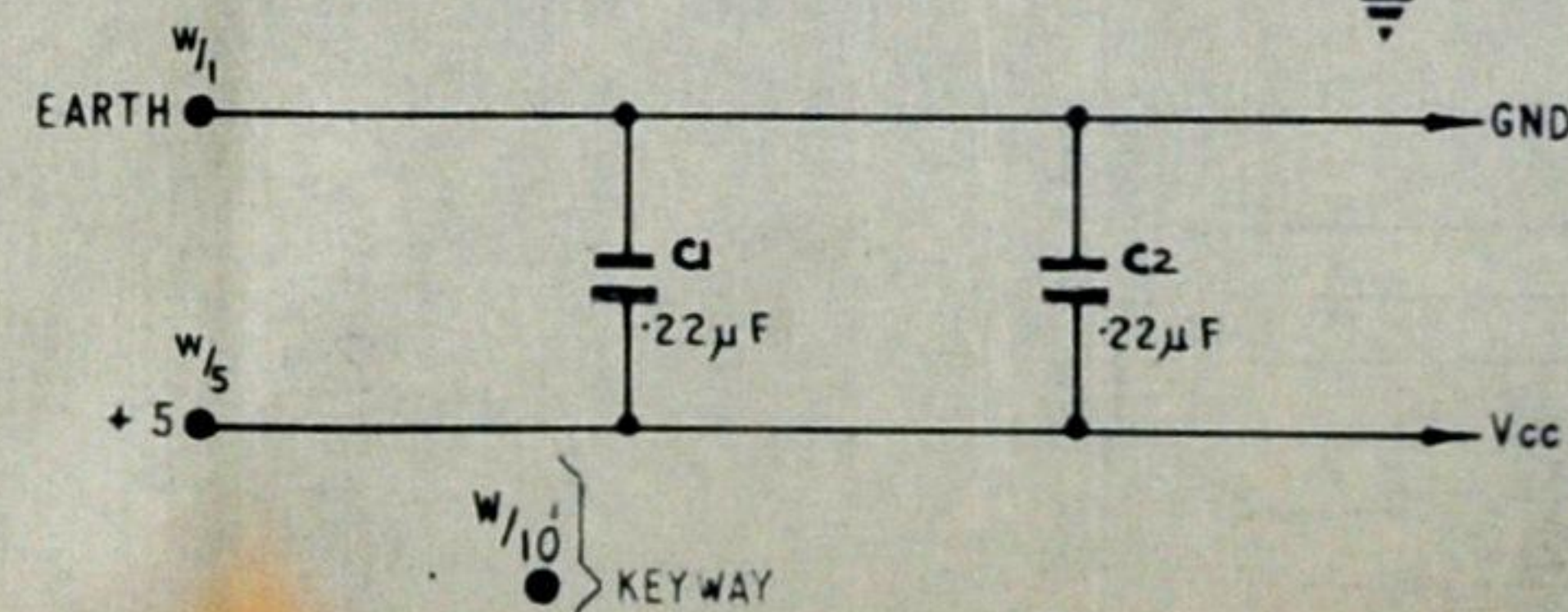
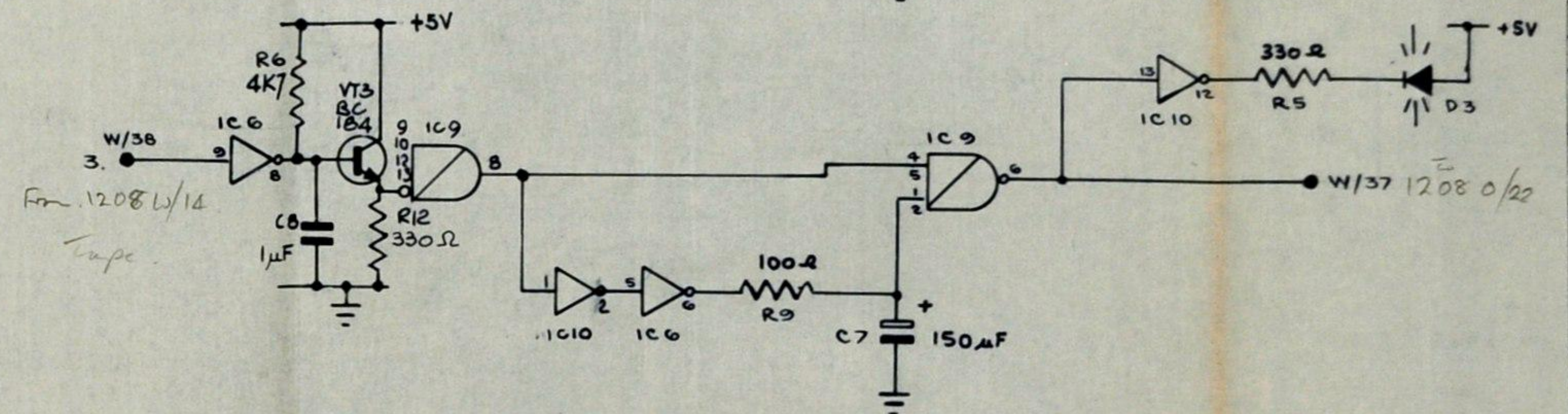
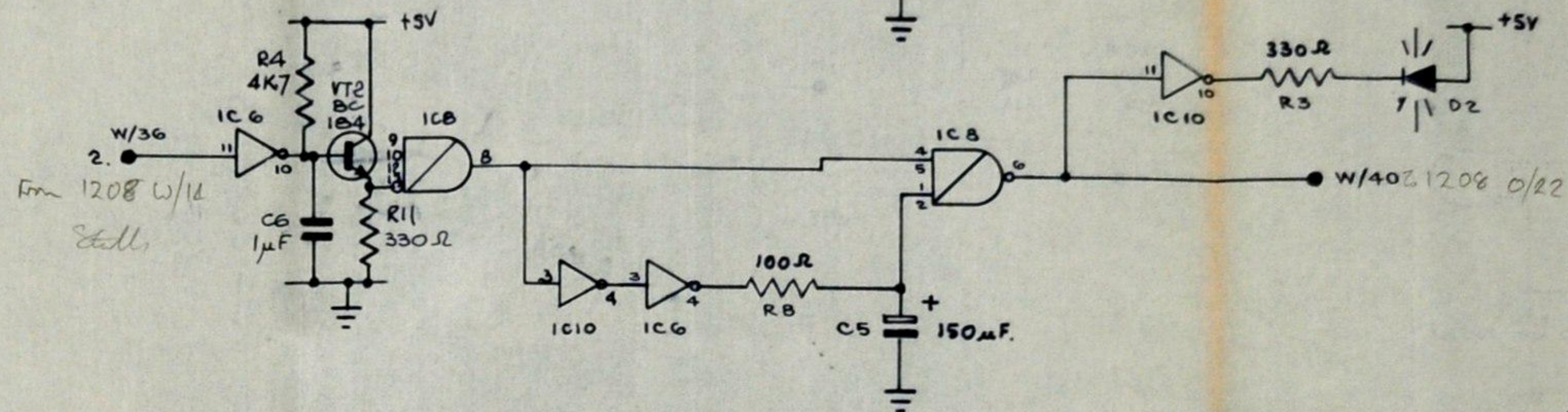
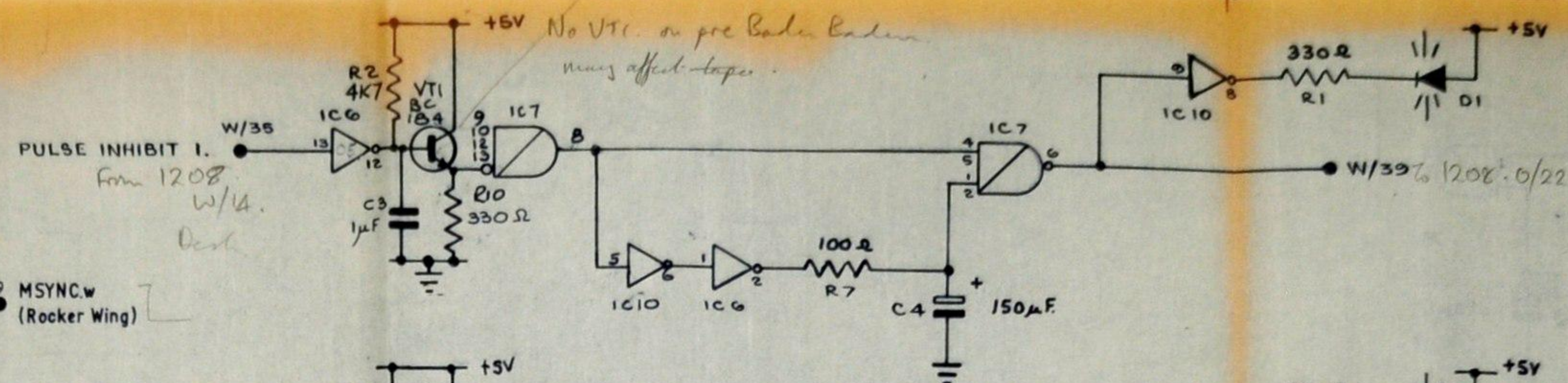
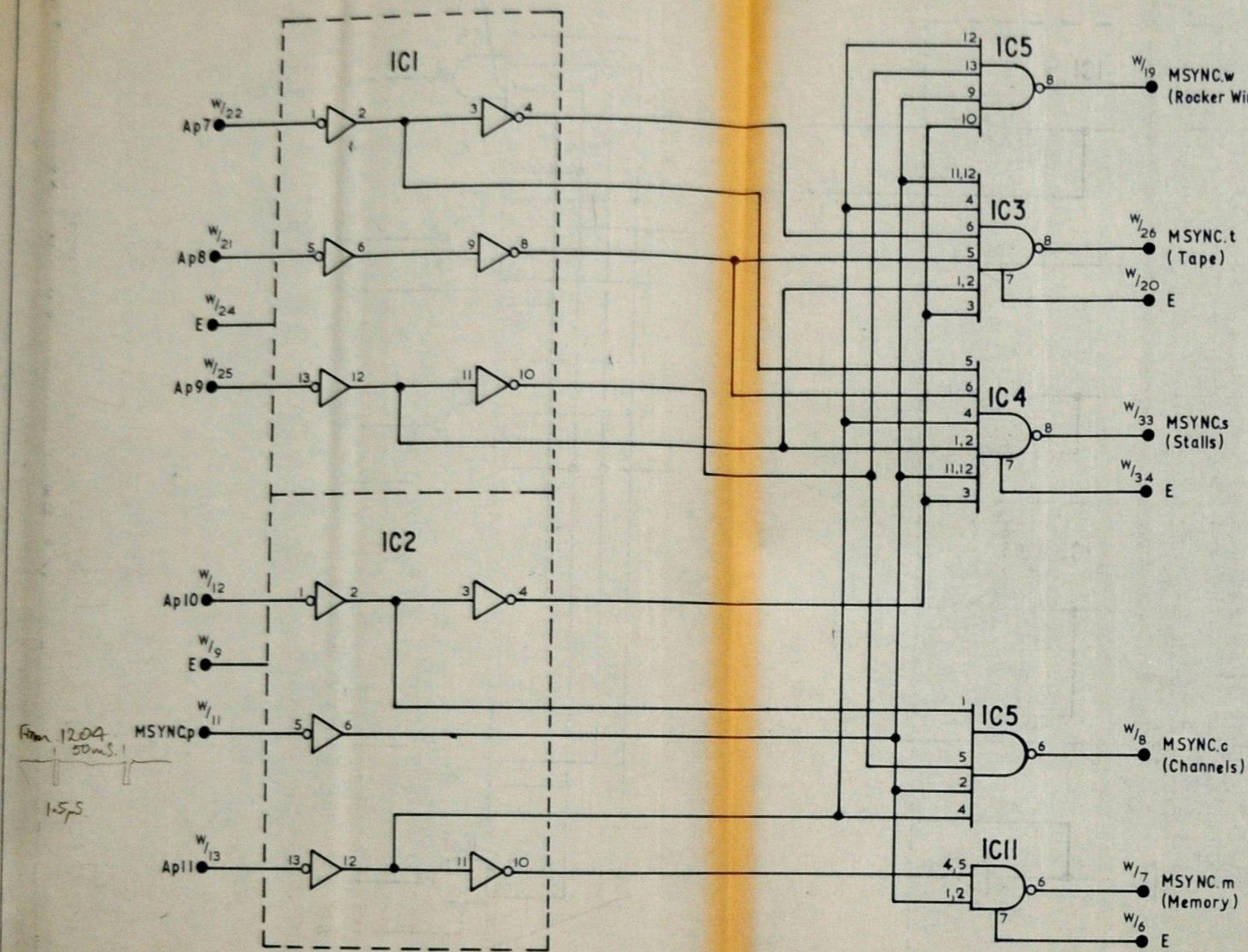
			<u>TITLE</u>
			DDM 2
D	13.9.72	R. Eason	Pdp DATA LINES INTERFACE.
C	14. 7. 72.	R. EASON	
B	3. 3. 72.	R. EASON	
A	20. 1. 72.	R. EASON	PCB 214/1
ISSUE	DATE	SIGNATURE	REF 1203
			DRG. NO. 6B01203



INTEGRATED CIRCUITS			
REF NO	TYPE	V _{cc}	GND
IC 13	SN7400N	PIN 14	PIN 7
IC 5	SN7401N	PIN 14	PIN 7
IC 3,8,9,12,	SN7404N	PIN 14	PIN 7
IC 15,	SN7410N	PIN 14	PIN 7
IC 4	SN7430N	PIN 14	PIN 7
IC 7	SN74L73N	PIN 4	PIN 11
IC 6	SN74L122N	" 14	" 7
IC 1,2,10,11,14,	SP380A	" 8	" 1

SCHEDULE: 5501228
P.C.B. DRG. 5801253

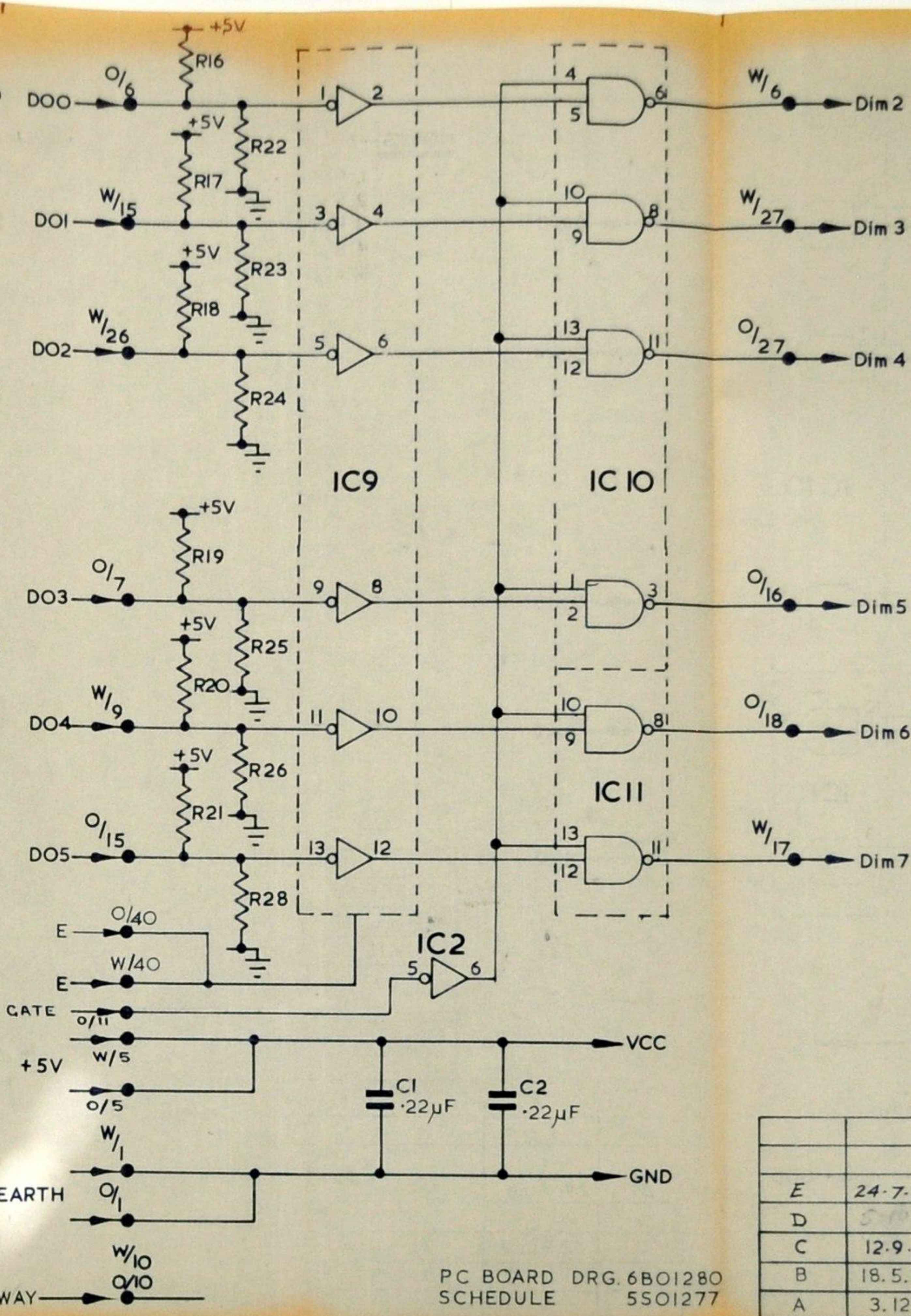
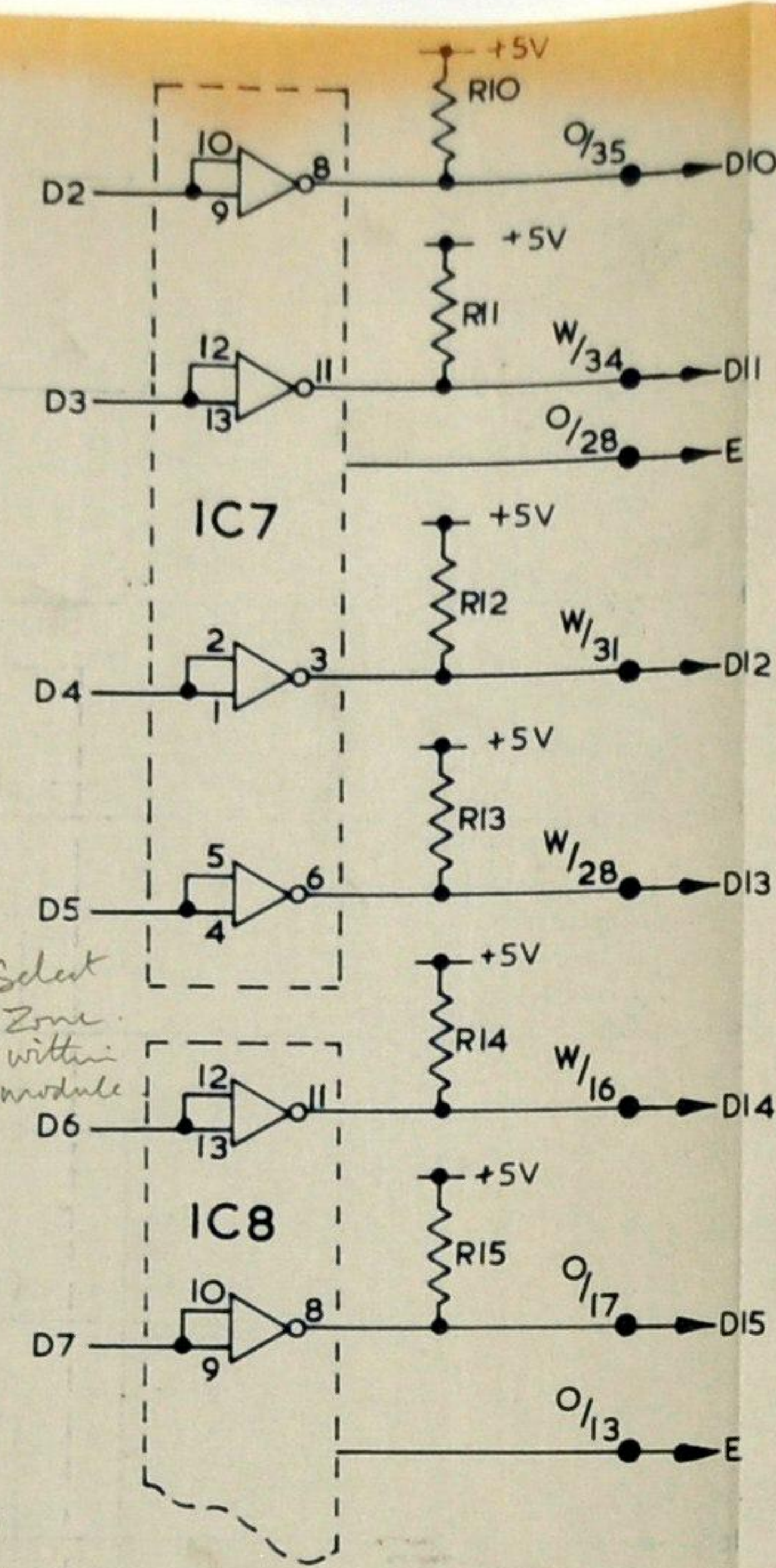
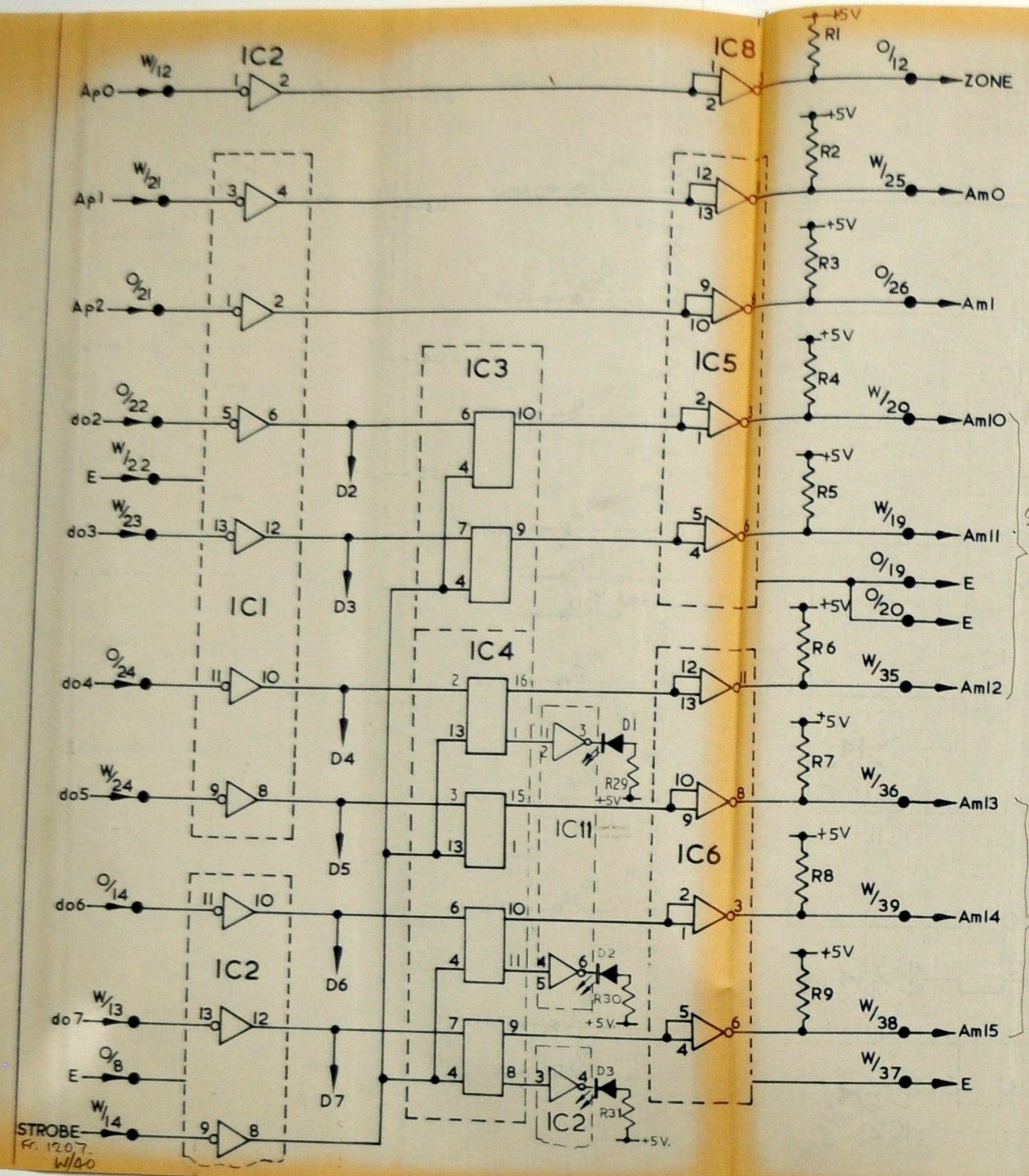
TITLE DDM 2			
Pdp ADDRESS LINE INTERFACE.			
C	20th Oct '72	R EASON	PCB 215/1 REF 1204
B	12.7.72	R EASON	DRG. NO. 6B01204.
A	15.3.72.	R EASON	



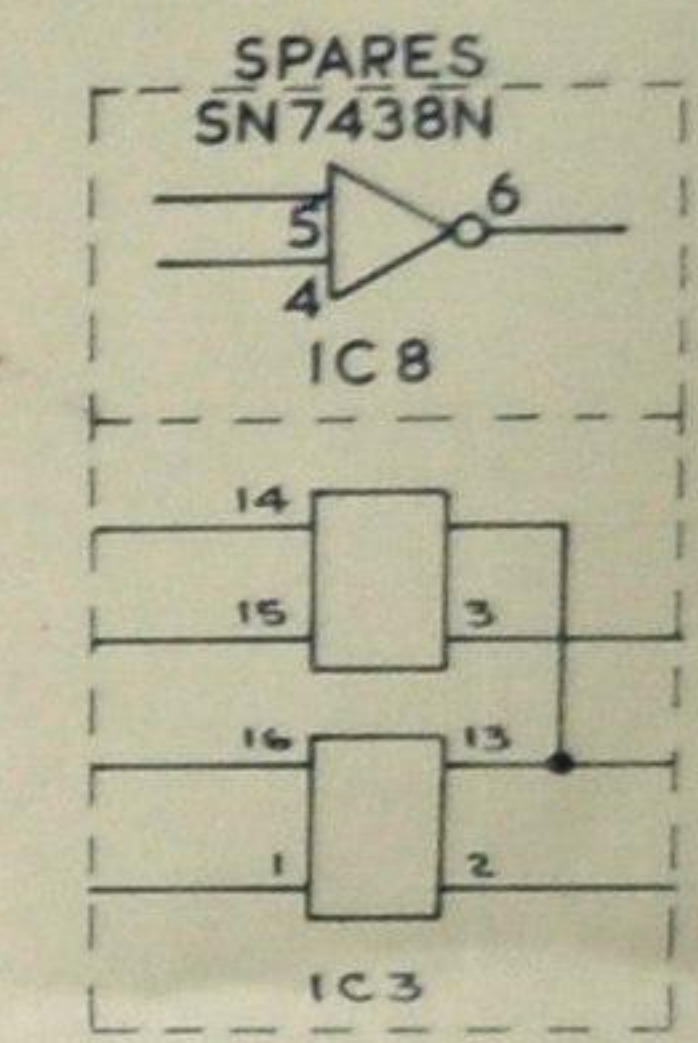
NOTE:-
1. ALL RESISTORS ARE 1/4W, 5%
UNLESS OTHERWISE STATED
2. PCB BOARD DWG. 5B01254
SCHEDULE DWG 5S01288

INTEGRATED CIRCUITS			
REF. No.	TYPE	+Vcc	GND
IC1, IC2 & IC10	SN7404N	Pin 14	Pin 7
IC6	SN7405N	Pin 14	Pin 7
IC7, 8, 9, 11	SN7413	Pin 14	Pin 7
IC5	SN7420	Pin 14	Pin 7
IC3 & IC4	SN7430	Pin 14	Pin 7

TITLE -			D.D.M.2	
			ADDRESS ZONING	
G	26-4-74	R. Eason	PCB 216/4	REF 1205
F	11-12-72	R. Eason		
E	30-5-72	R. Eason	DRG No. 6B01205	
ISSUE	DATE	SIGNATURE		



- NOTES:-
1. RESISTORS R1 TO R15 ARE 510Ω 2%.
 2. RESISTORS R16 TO R21 ARE 390Ω.
 3. RESISTORS R22 TO R26, R28 ARE 470Ω.
 4. RESISTORS R29, R30, R31 ARE 330Ω.
 5. ALL DIODES ARE TEXAS TIL 209



INTEGRATED CIRCUITS			
REF No.	TYPE	Vcc	GND
IC 1,2,9	SN7404N	Pin 14	Pin 7
IC 10 & 11	SN7400N	Pin 14	Pin 7
IC 5,6,7 & 8	SN7438N	Pin 14	Pin 7
IC 3 & 4	SN74L75N	Pin 5	Pin 12

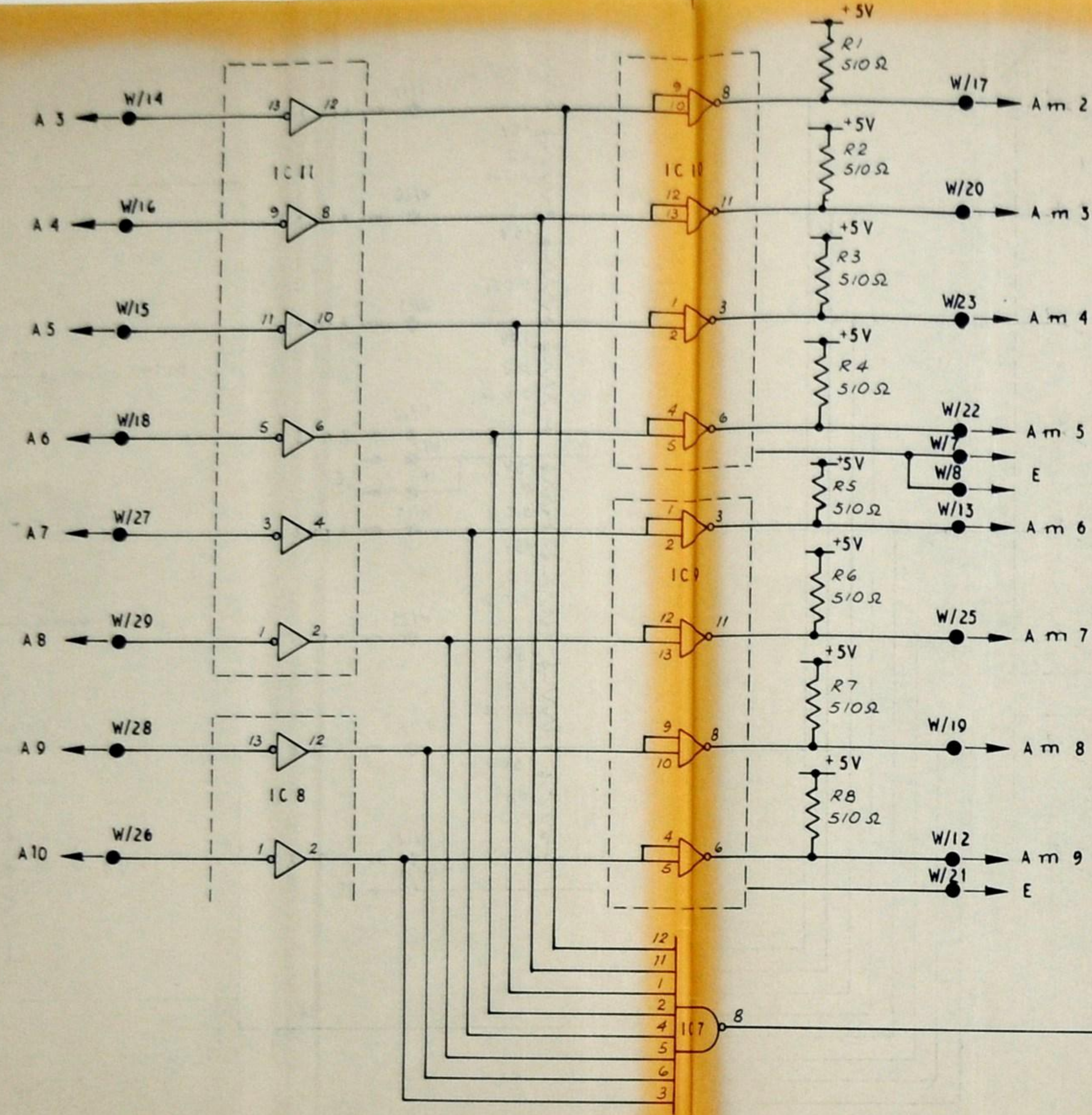
TITLE
MEMORY ADDRESS &
DATA LINE INTERFACE.

E	24.7.73	
D		
C	12.9.72	
B	18.5.72.	R.EASON
A	3.12.72.	
ISSUE	DATE	SIGNATURE

PCB 217 REF 1206
DRG. No. 6B01206

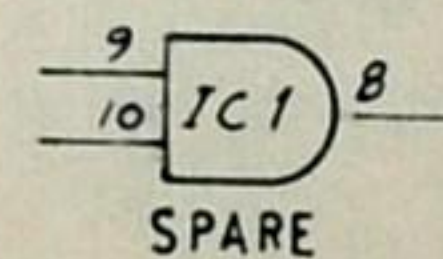
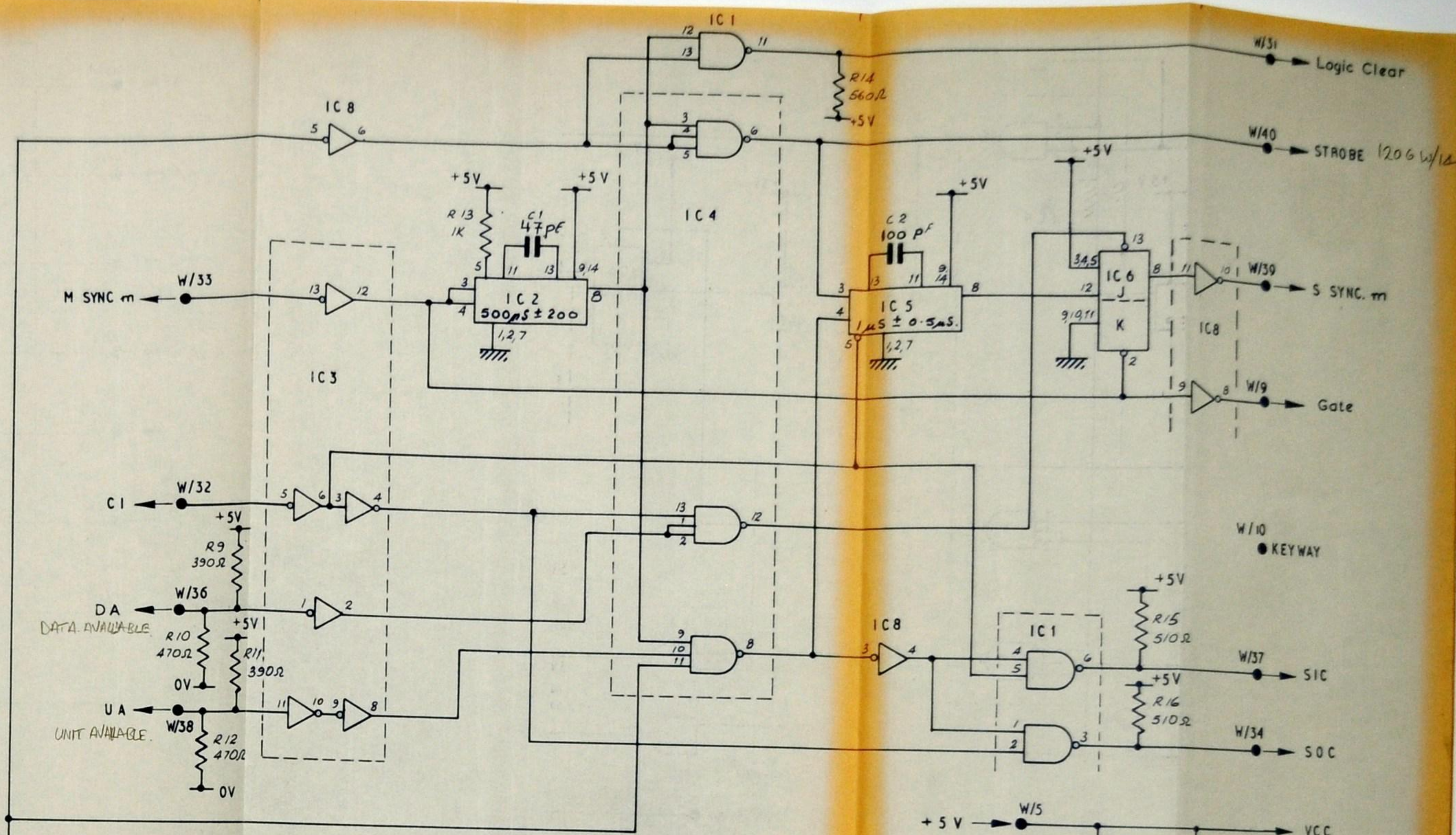
PC BOARD DRG. 6B01280
SCHEDULE 5501277

Select module.
Uniform address
lines address within
module zone.

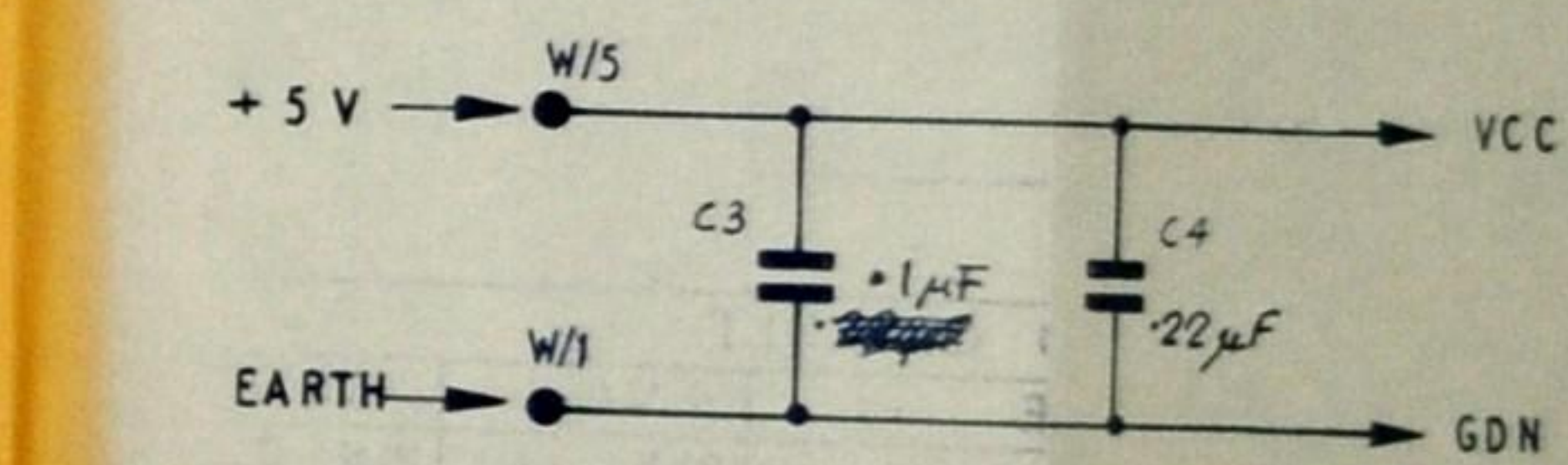


PC BOARD DRG No 6B01256

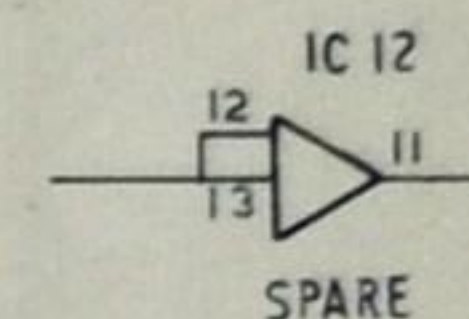
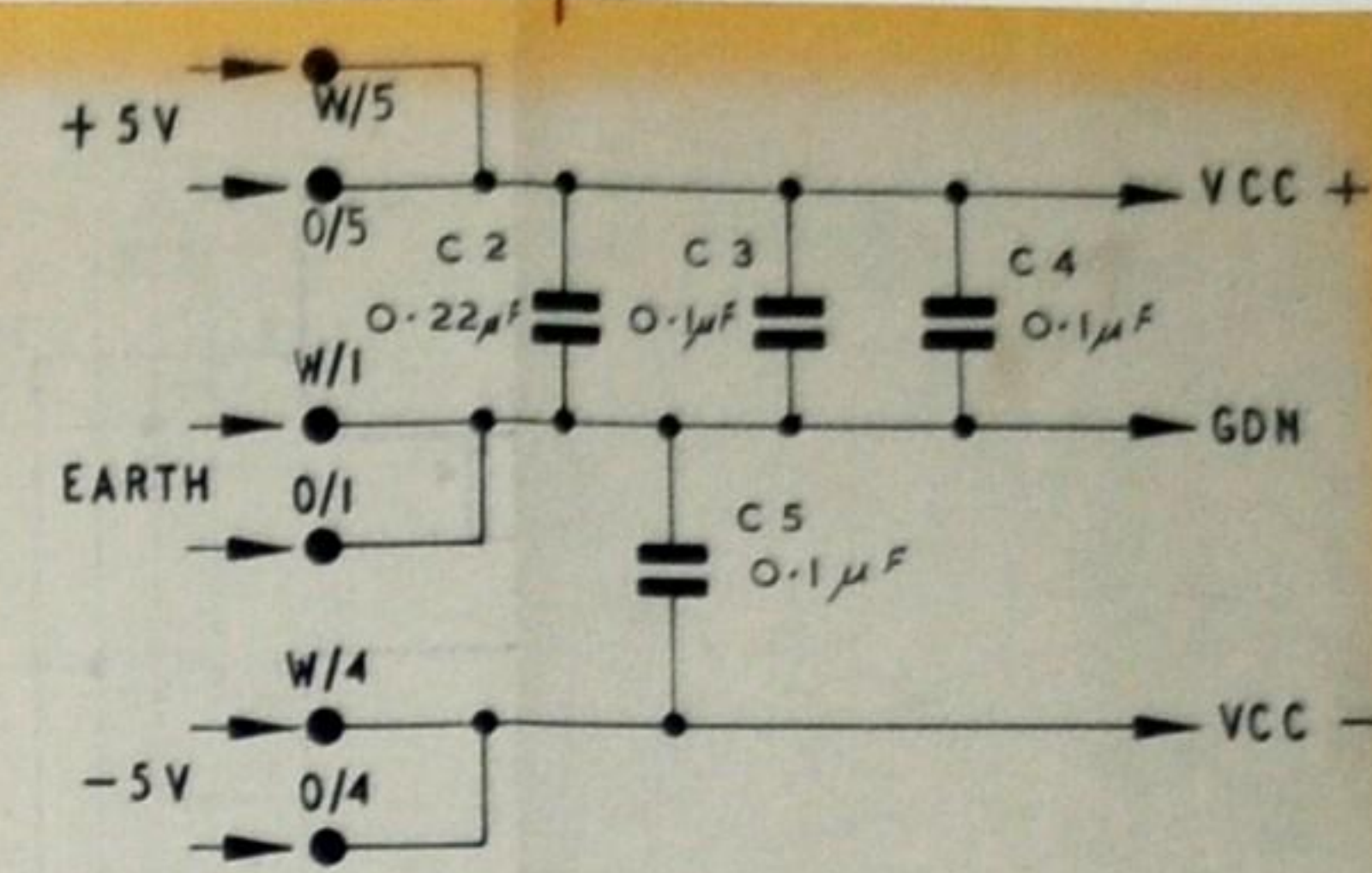
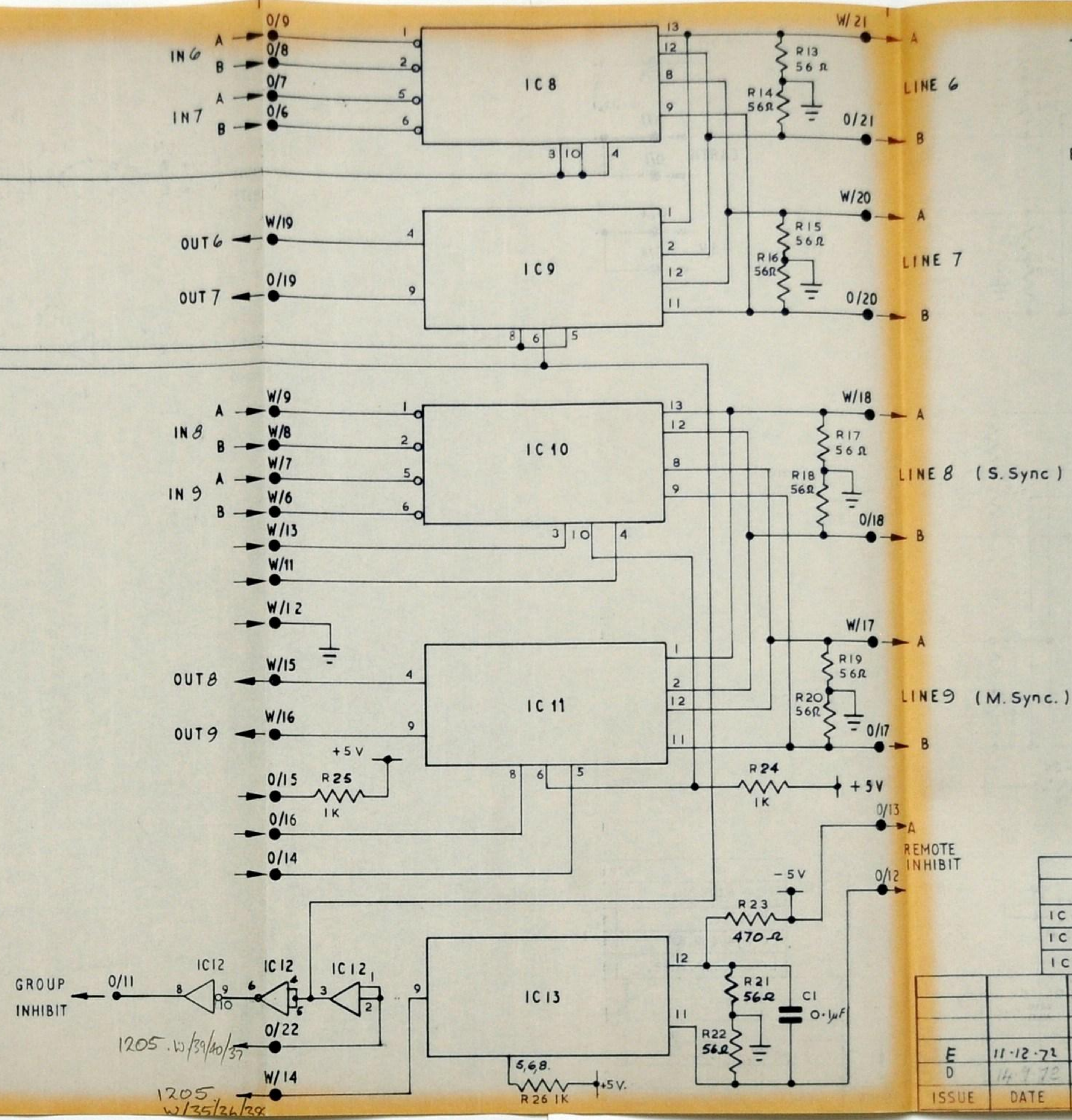
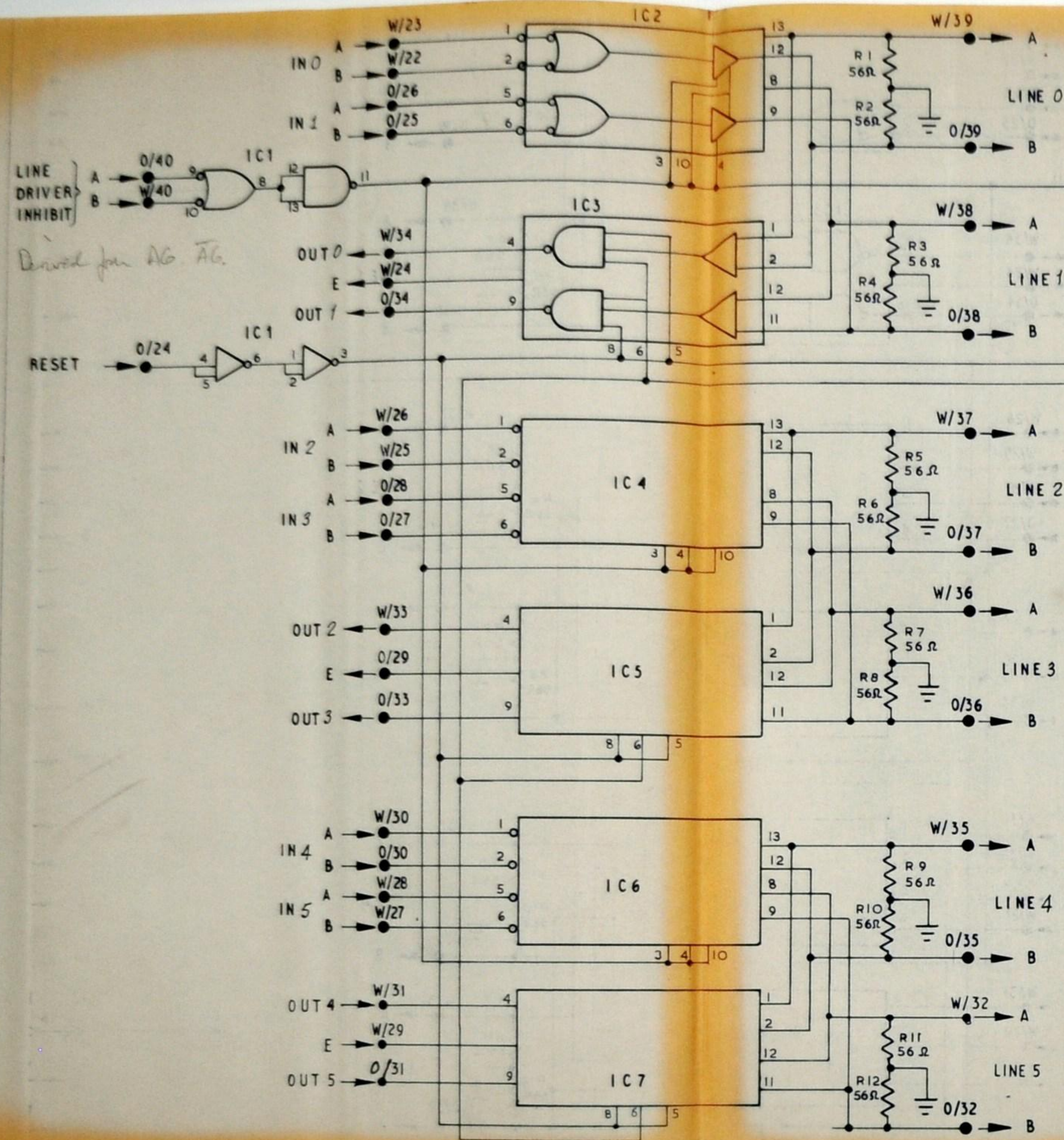
SCHEDULE 5501231



INTEGRATED CIRCUIT			
REF No	TYPE	+VCC	GDN.
IC1, 9, 10	SN 7438 N	PIN 14	PIN 7
IC2, 5	SN 74L122 N	" 14	" 7
IC3, 8, 11	SN 7404 N	" 14	" 7
IC4	SN 7410 N	" 14	" 7
IC6	SN 7472 N	" 14	" 7
IC7	SN 7430 N	" 14	" 7



TITLE:-			
MEMORY CONTROL & ADDRESS LINE INTERFACE CIRCUIT DIAGRAM			
D	11-12-72	R. E. S.	PCB 218
C	7-9-72	R. E. S.	REF 1207
ISSUE	DATE	SIGNATURE	DRG. No 6B01207



ALL RESISTORS ARE 1/4W 2%
UNLESS OTHERWISE STATED.

PC BOARD DRG 5B01257

SCHEDULE 55 01232

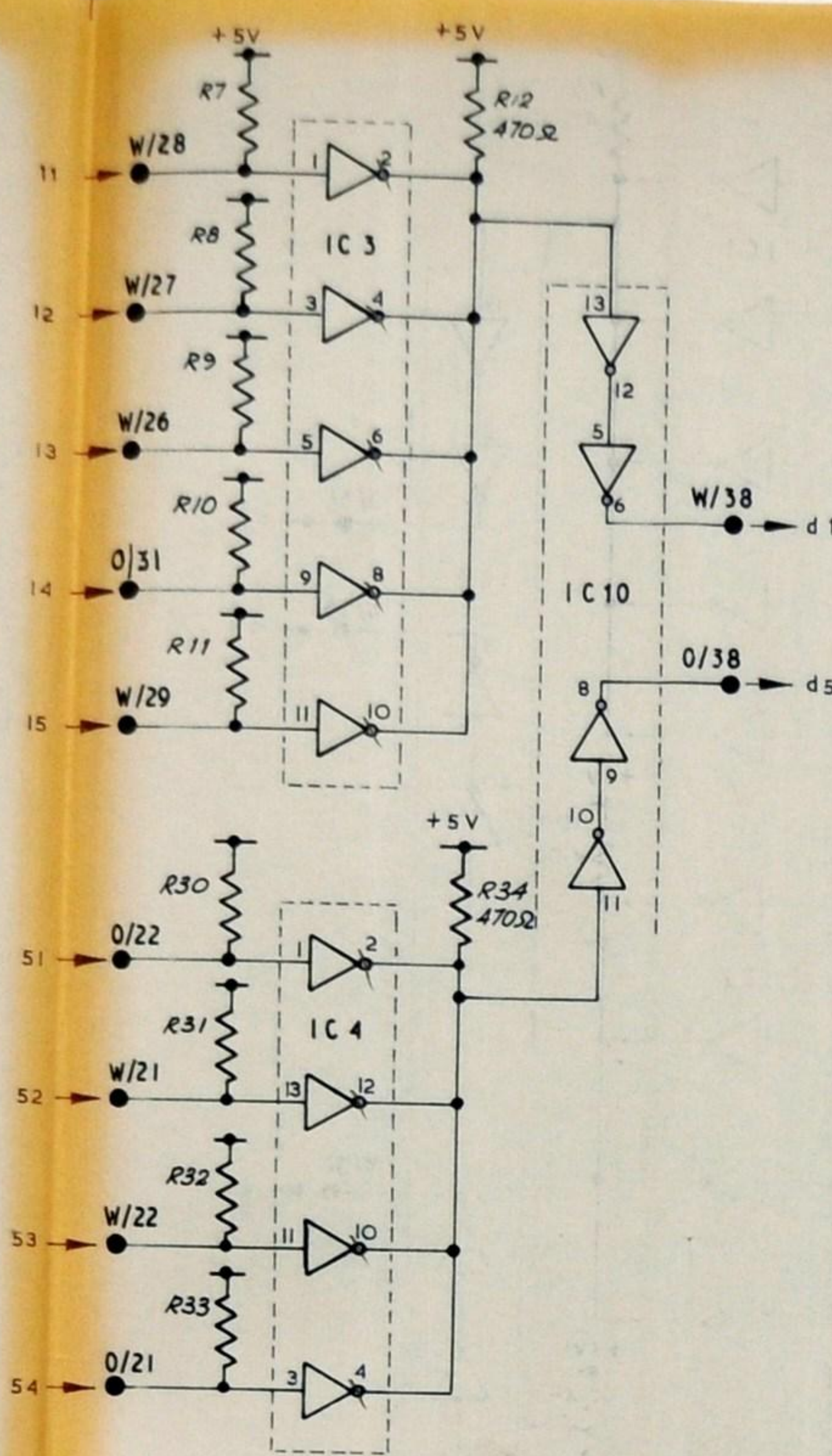
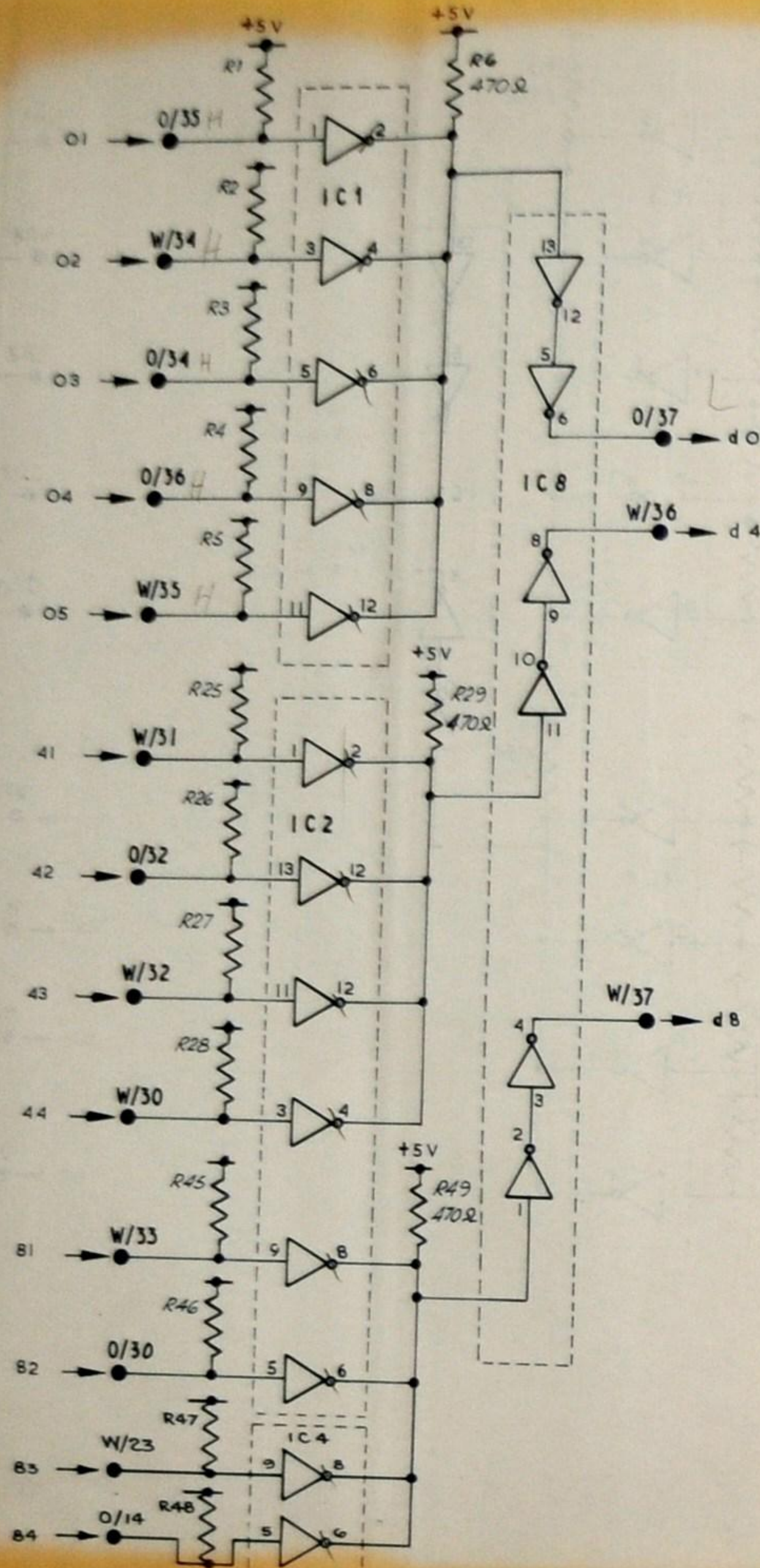
INTEGRATED CIRCUITS				
REF. No	TYPE	VCC +	VCC -	GND
IC 1, 12.	SN7437N	PIN 14	---	PIN 7
IC 2, 4, 6, 8, 10.	SN75110N	" 14	PIN 11	" 7
IC 3, 5, 7, 9, 11, 13.	SN75107N	" 14	" 13	" 7

DDM 2
LINE DRIVER & RECEIVER
LOGIC DIAGRAM.

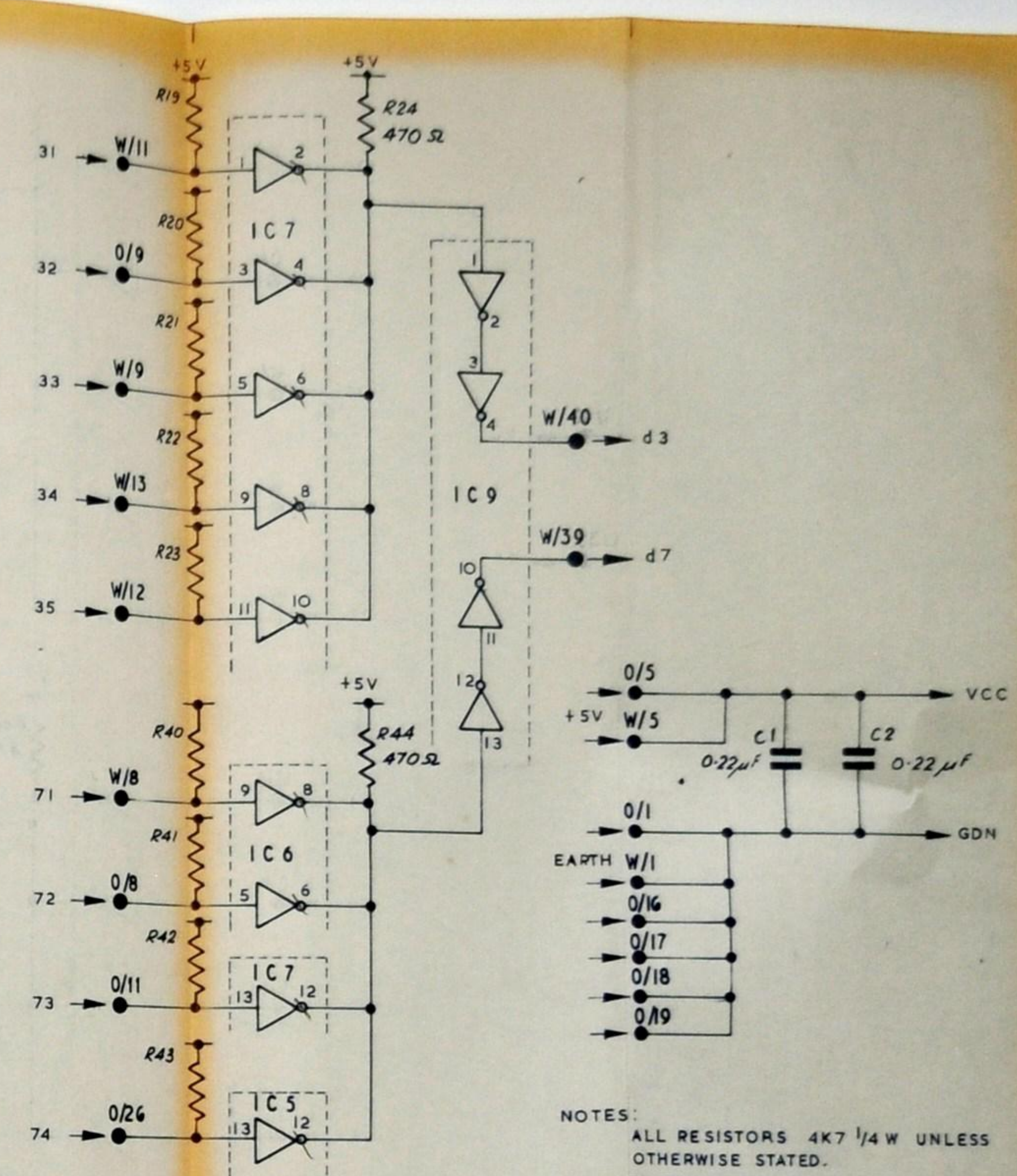
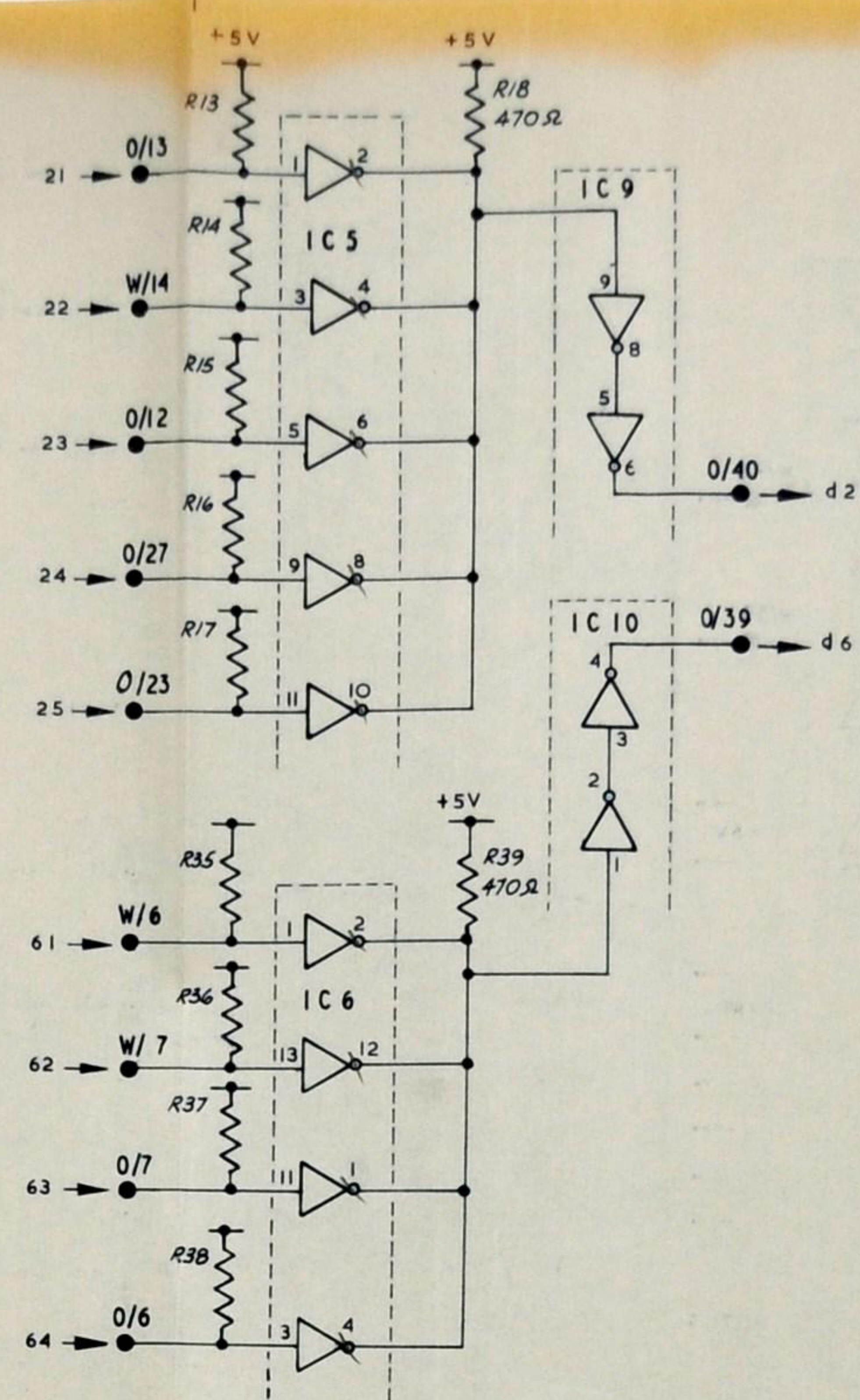
ISSUE	DATE	SIGNATURE
E	11-12-72	R. Brown
D	14-7-72	R. Brown

PCB 219/1
DRG NO.

REF 1208
6B01208



KEY WAY
 ● W/10
 ● O/10

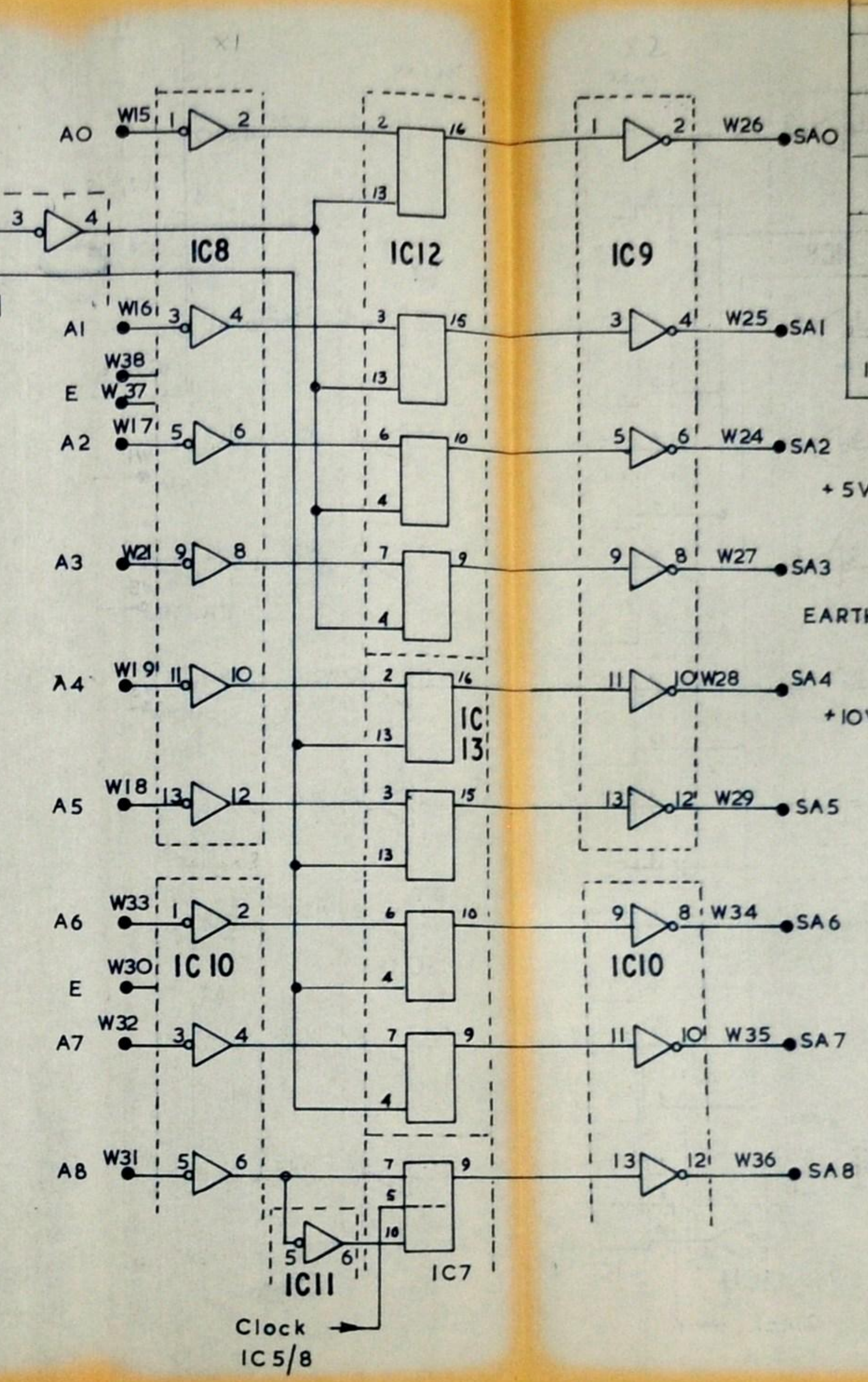
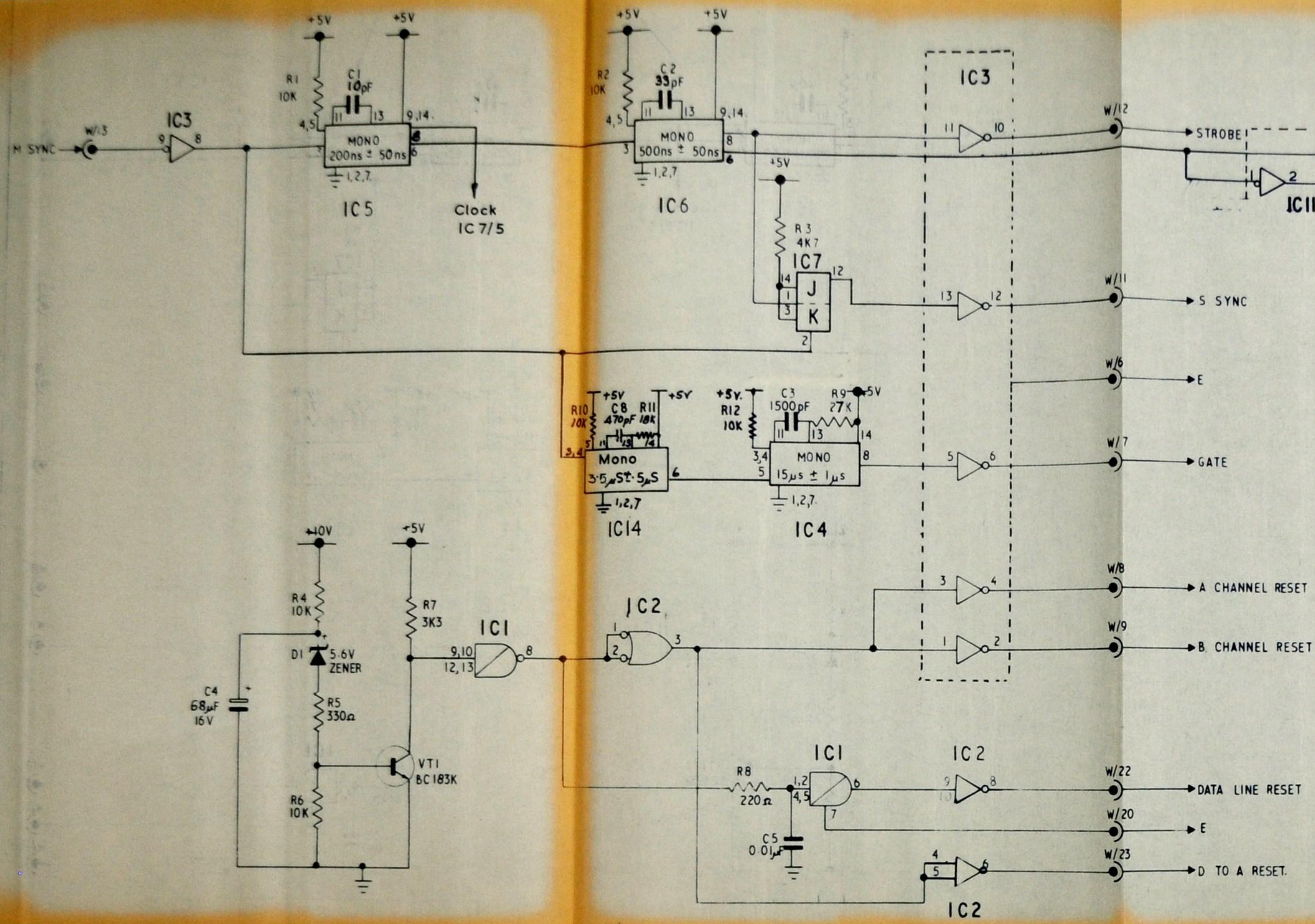


NOTES:
 ALL RESISTORS 4K7 1/4W UNLESS OTHERWISE STATED.
 PC BOARD DWG. 5B01258
 SCHEDULE 5501233

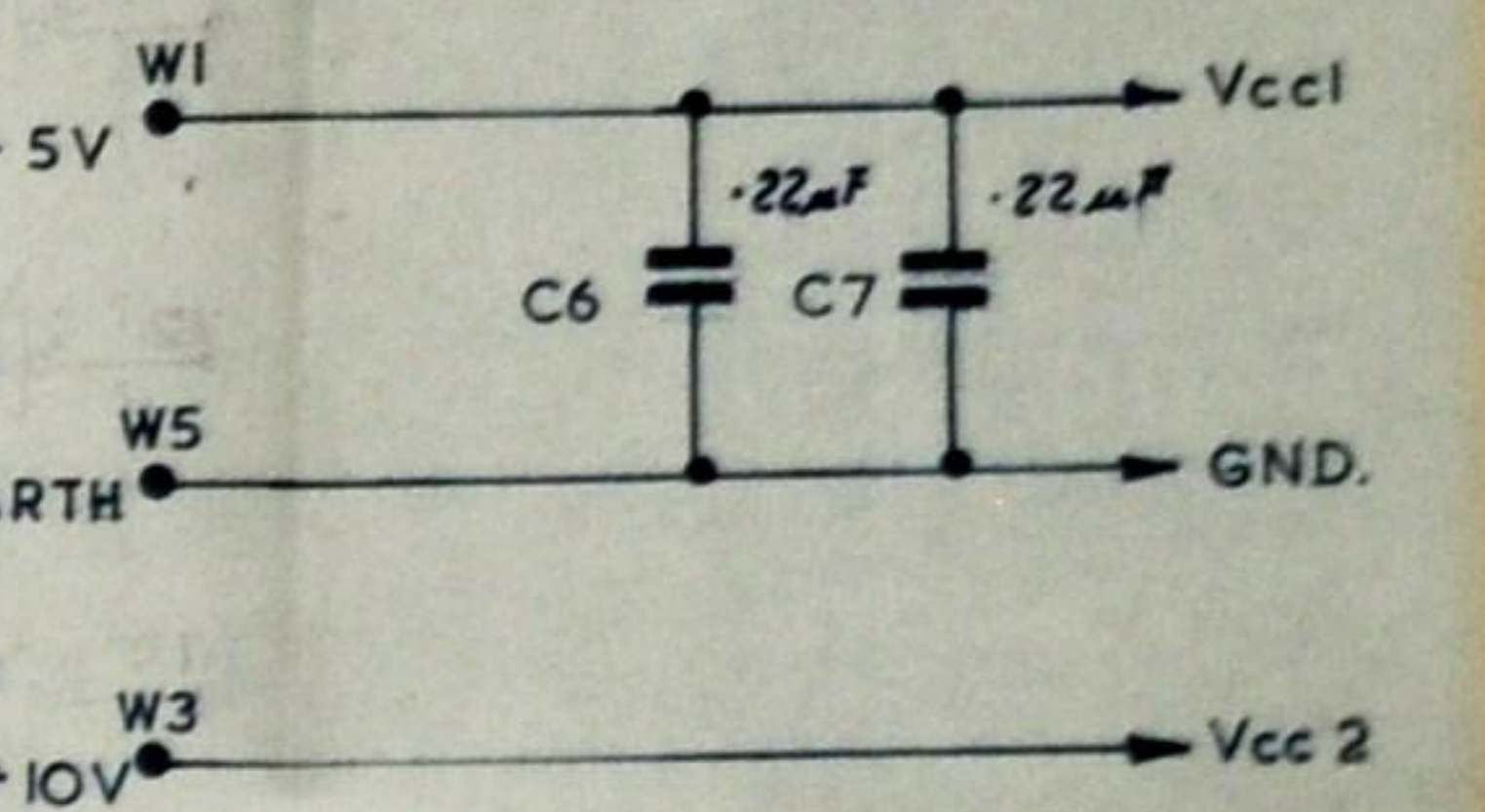
N.B. NON INVERTING

INTEGRATED CIRCUITS			
REF. N°	TYPE	Vcc	GDN
IC 1, 2, 3, 4, 5, 6, 7	SN7417N	14	7
IC 8, 9, 10	SN7404N	14	7

			TITLE :- DDM 2 'OR' GATE LOGIC DIAGRAM. REF. 1209 PCB 220 DWG N° 6BO1209
C	11.7.73	<i>R. Eason</i>	
B	11.12.72	<i>R. Eason</i>	
ISSUE	DATE	SIGNATURE	



REF No	TYPE	Vcc	GND
IC1	SN 7413N	Pin 14	Pin 7
IC2	SN 7400N	14	7
IC3, 8, 9, 10 & 11	SN 7404N	14	7
IC4, IC5, IC6, IC7	SN 74L122N	14	7
IC7	SN 74L73N	4	11
IC12 & IC13	SN74L75	5	12

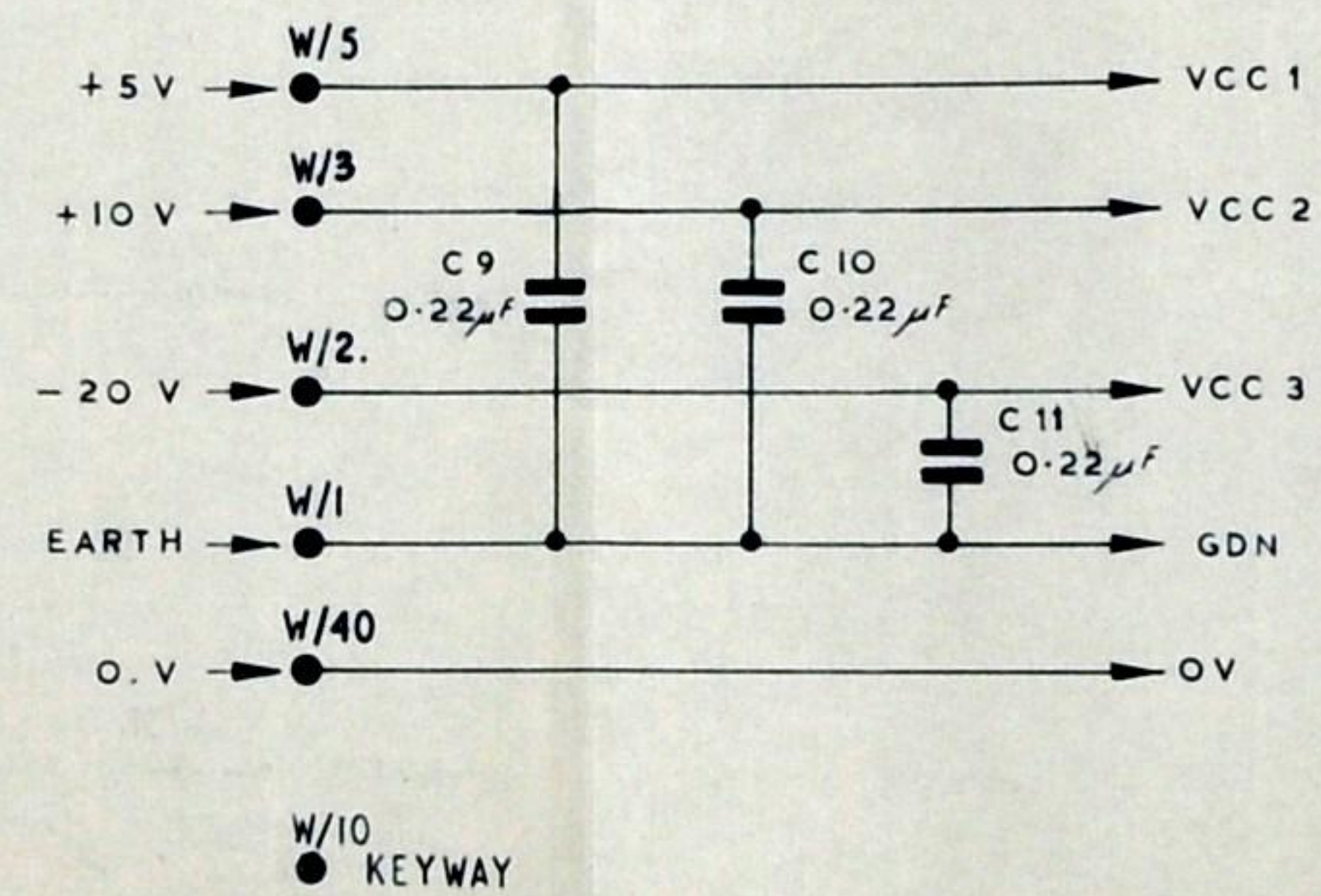
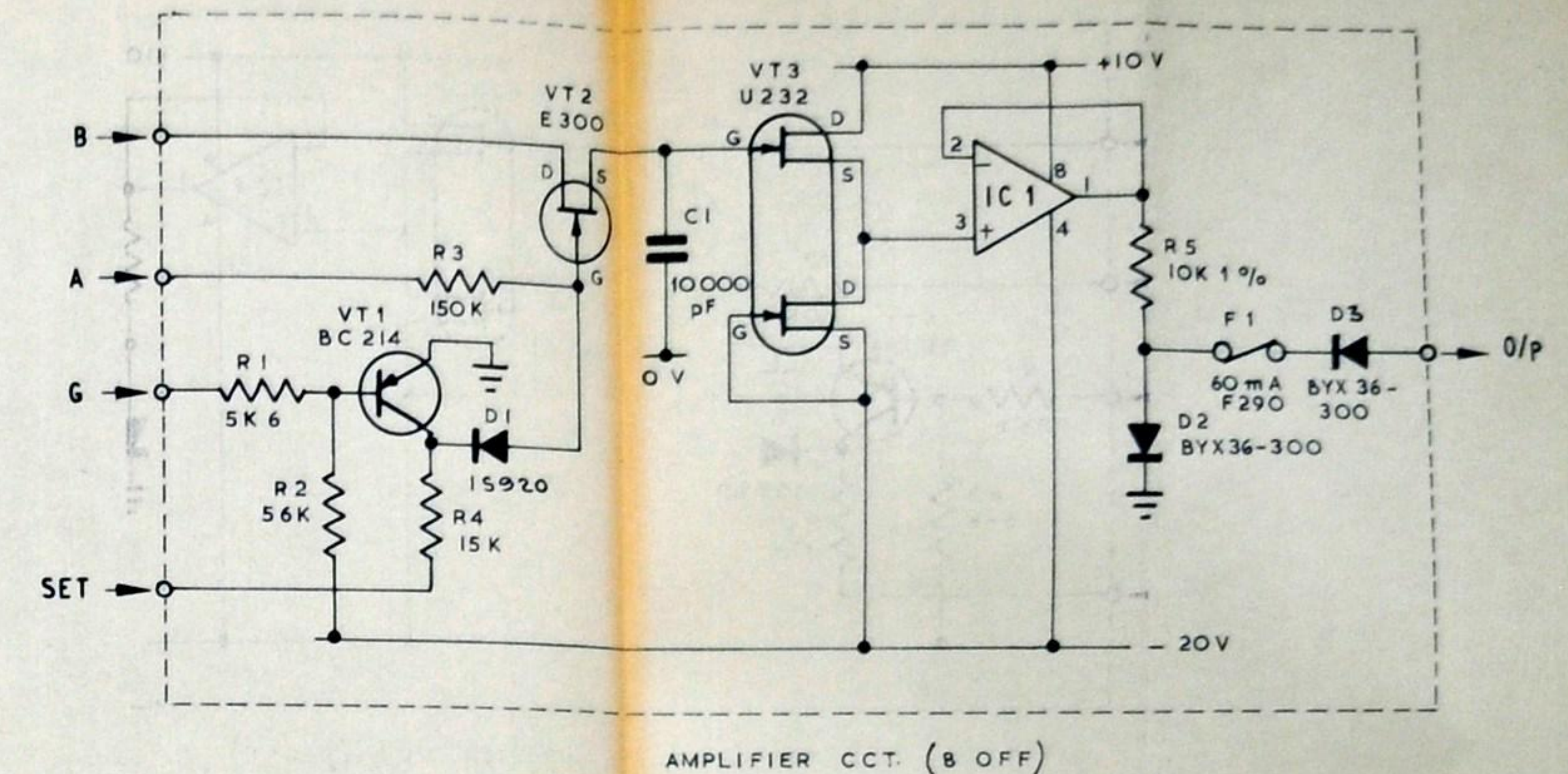
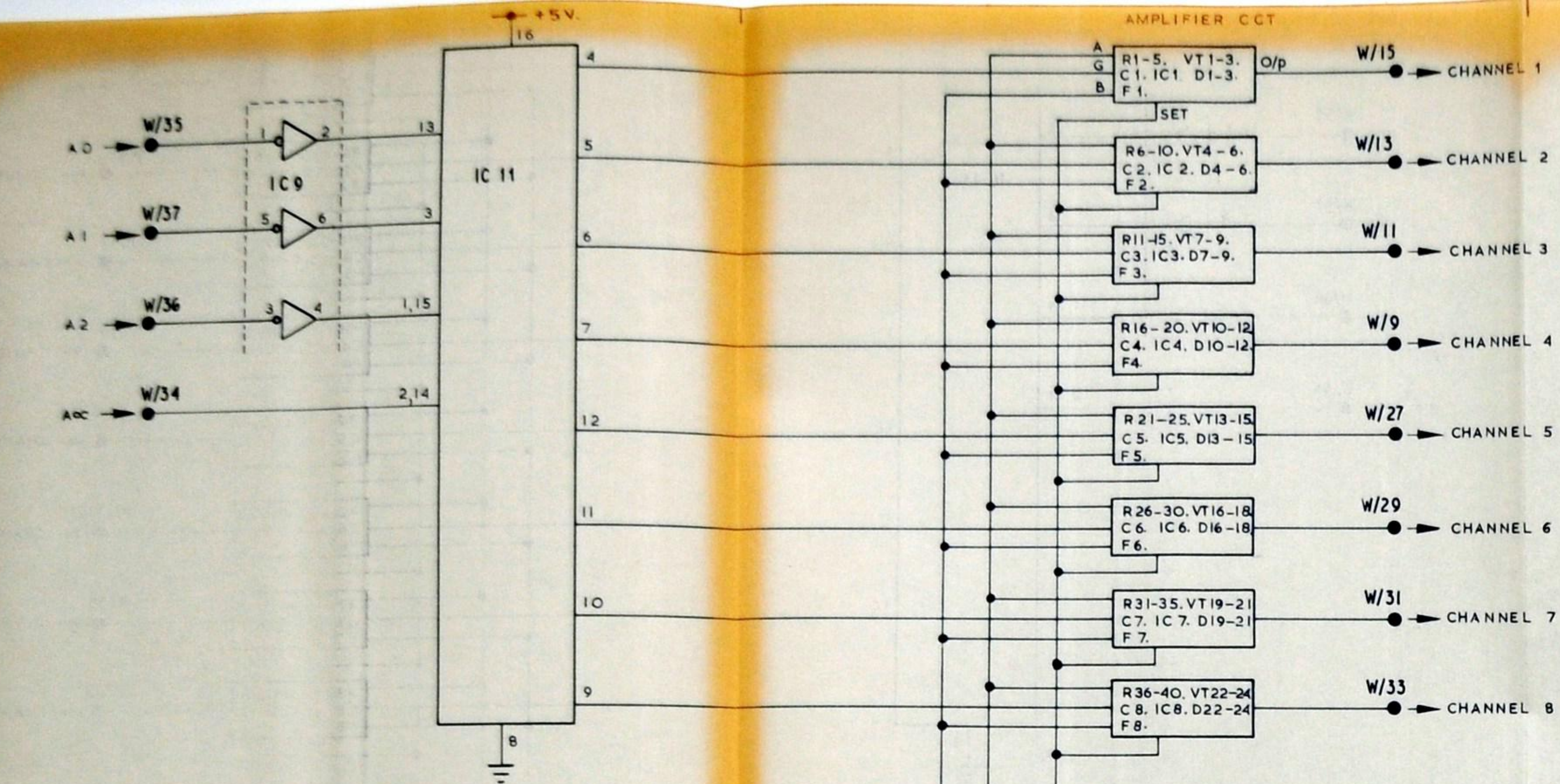


Note.

1. All resistors are 1/3 Watt 5% Unless otherwise stated.
2. PC Board Drg. No 5801259 Schedule Drg. No. 5501234

J	DATE	SIGNATURE
9.11.72		
31.10.72		
25.10.72		
ISSUE	DATE	SIGNATURE

DDM 2
SAMPLE & HOLD CONTROL
PCB 221/4
DRG No. 6B 01210
REF 1210



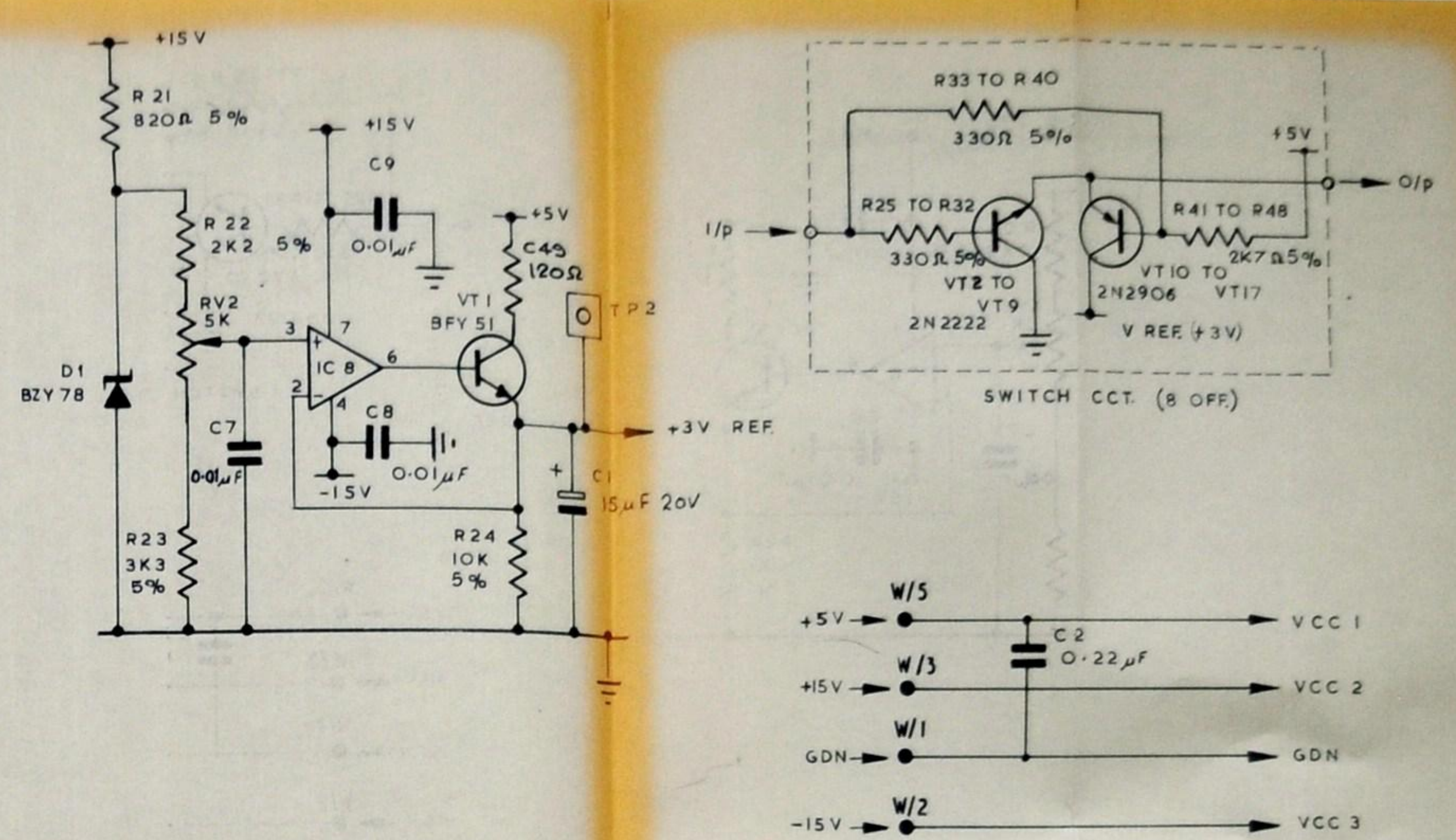
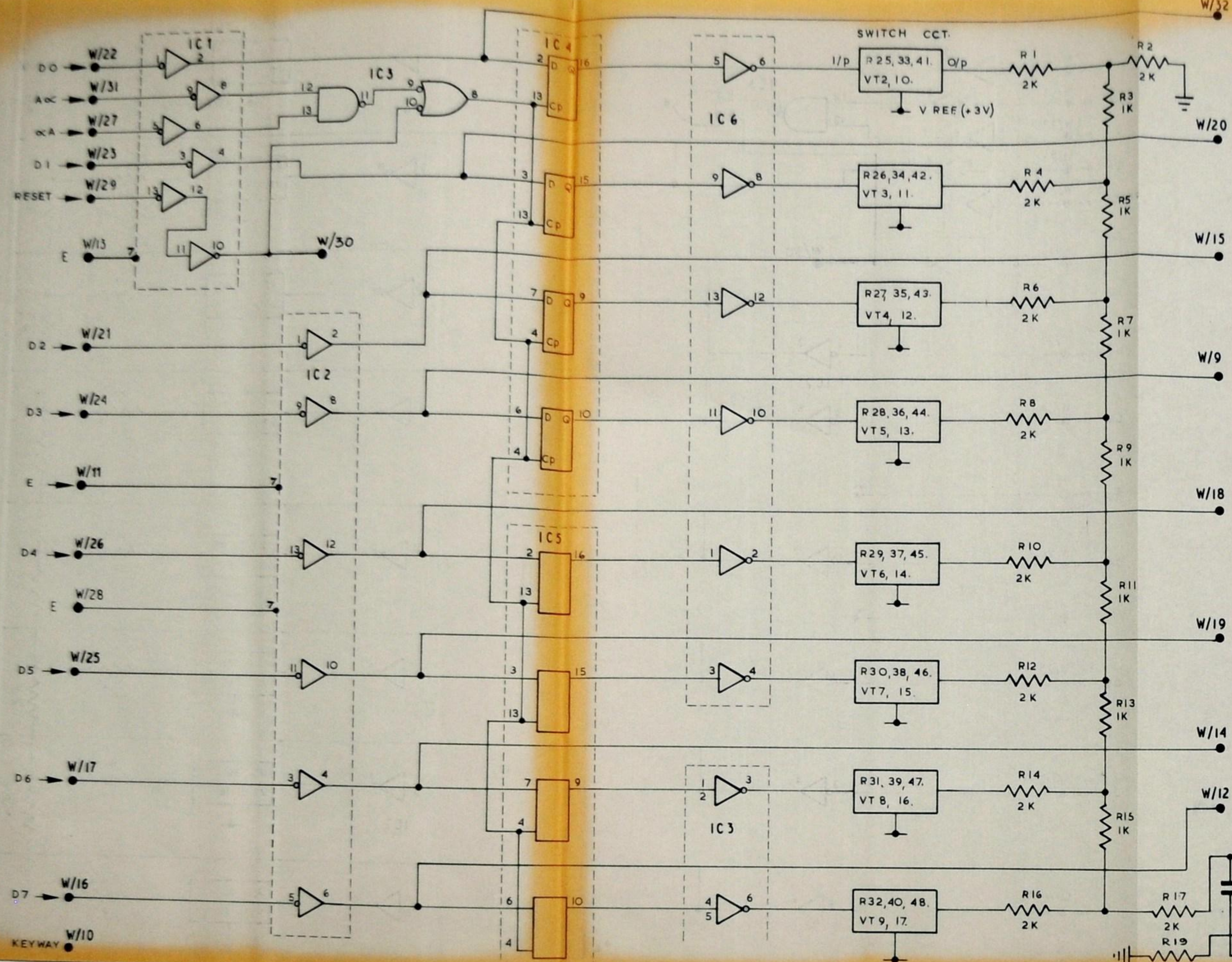
INTEGRATED CIRCUITS.					
REF. No.	TYPE	VCC 1	VCC 2	VCC 3	GDN.
IC 1-IC 8	SN 72741P	—	PIN 8	PIN 4	—
IC 9	SN 74L04	PIN 14	—	—	PIN 7
IC 10	LM 310D	—	PIN 11	PIN 6	—
IC 11	SN 74155N	PIN 16	—	—	PIN 8

NOTE.
ALL RESISTORS ARE 1/4 W 5%
UNLESS OTHERWISE STATED.

P.C. BOARD DRG. 5801260

SCHEDULE 5501235

TITLE			D.D.M. 2.	
8 CHANNEL SAMPLE & HOLD			LOGIC DIAGRAM.	
PCB 222			REF 121	
ISSUE	DATE	SIGNATURE	DWG. No 6801211	
B	11-12-72	R. R. R.		



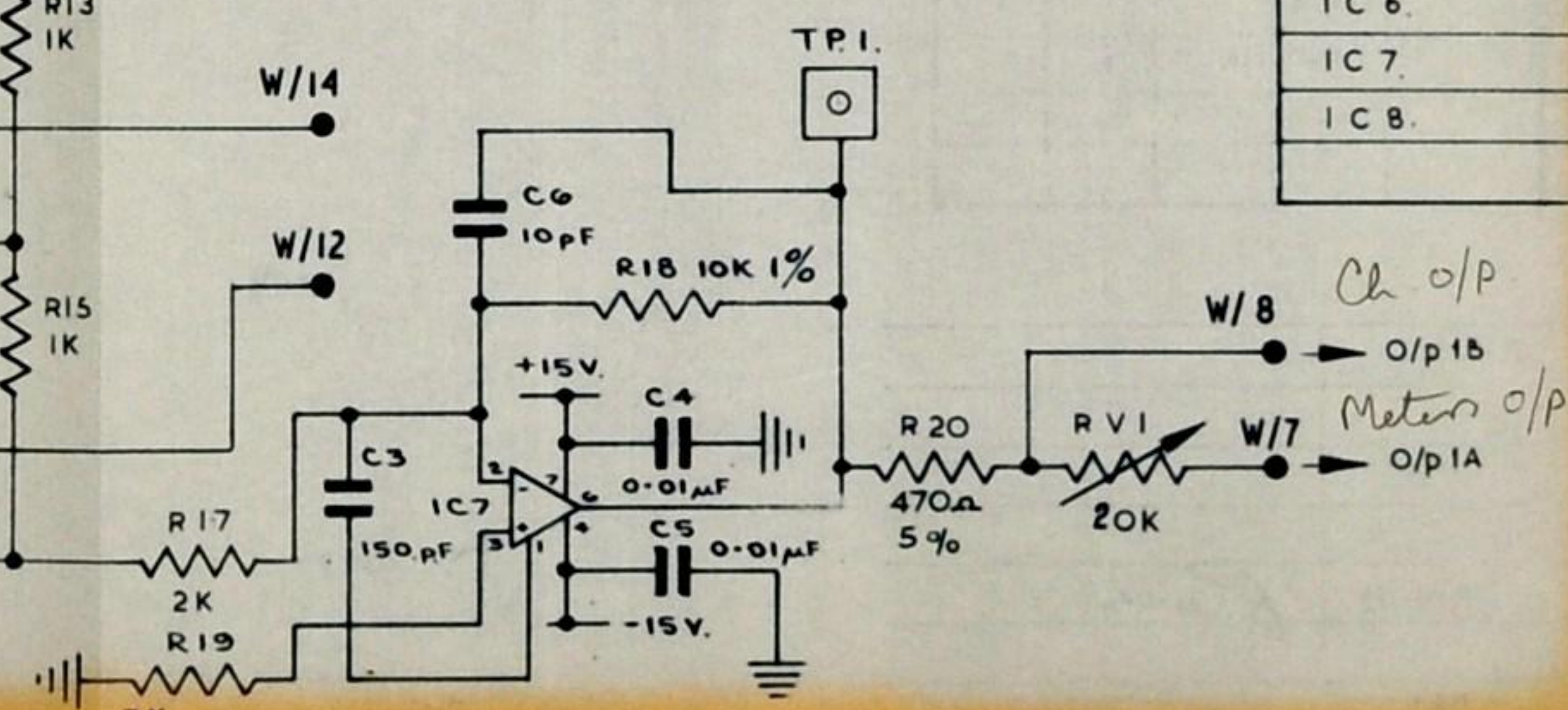
INTEGRATED CIRCUITS					
REF No.	TYPE	VCC1	VCC2	VCC3	GDN
IC 1, 2	SN 74LO4N	PIN 14	—	—	PIN 7
IC 3	SN 7400N	" 14	—	—	" 7
IC 4, 5	SN 74L75N	" 5	—	—	" 12
IC 6	SN 7404N	" 14	—	—	" 7
IC 7	SN 72301AP	—	PIN 7	PIN 4	—
IC 8	SN 72741P	—	" 7	" 4	—

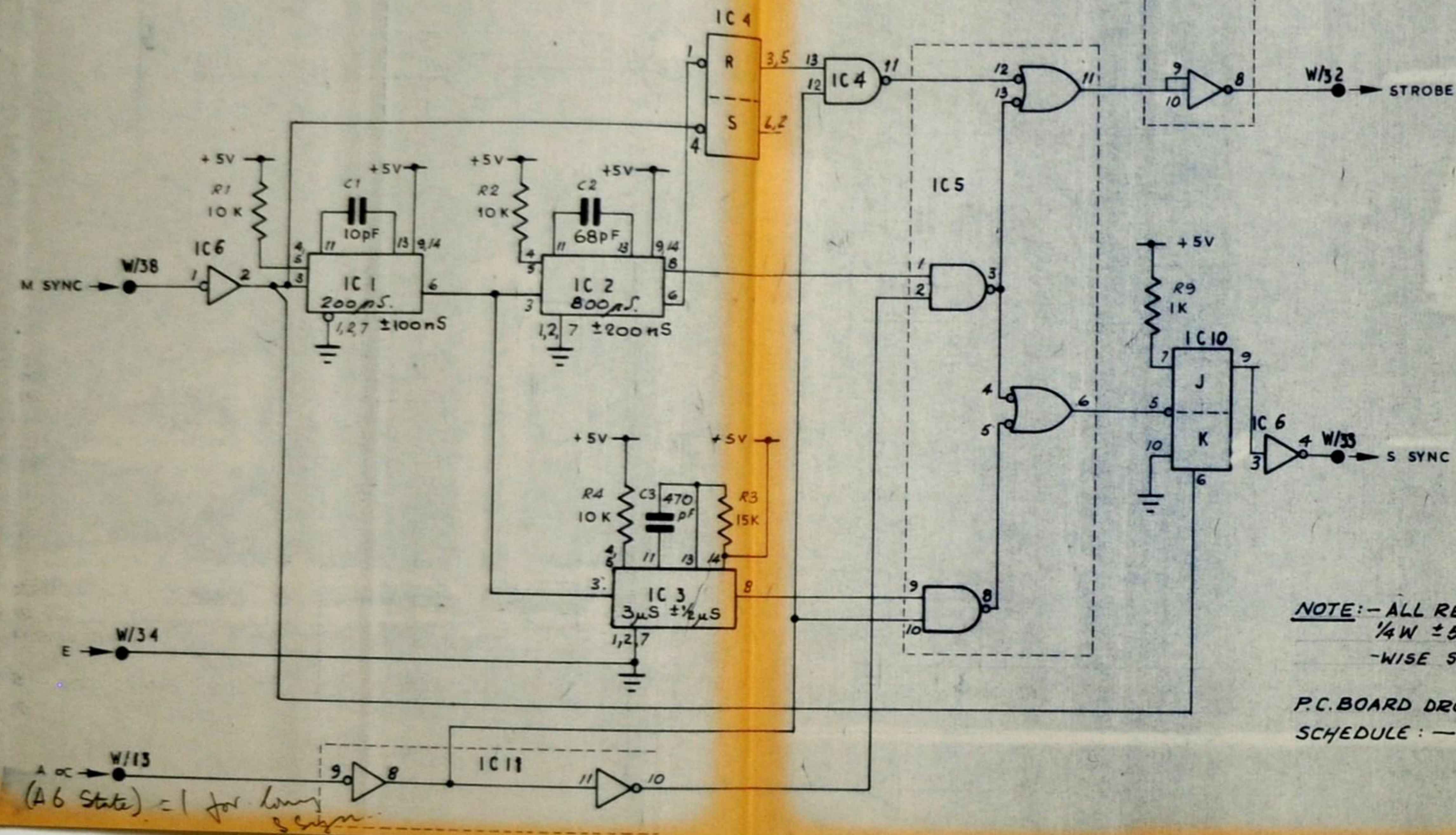
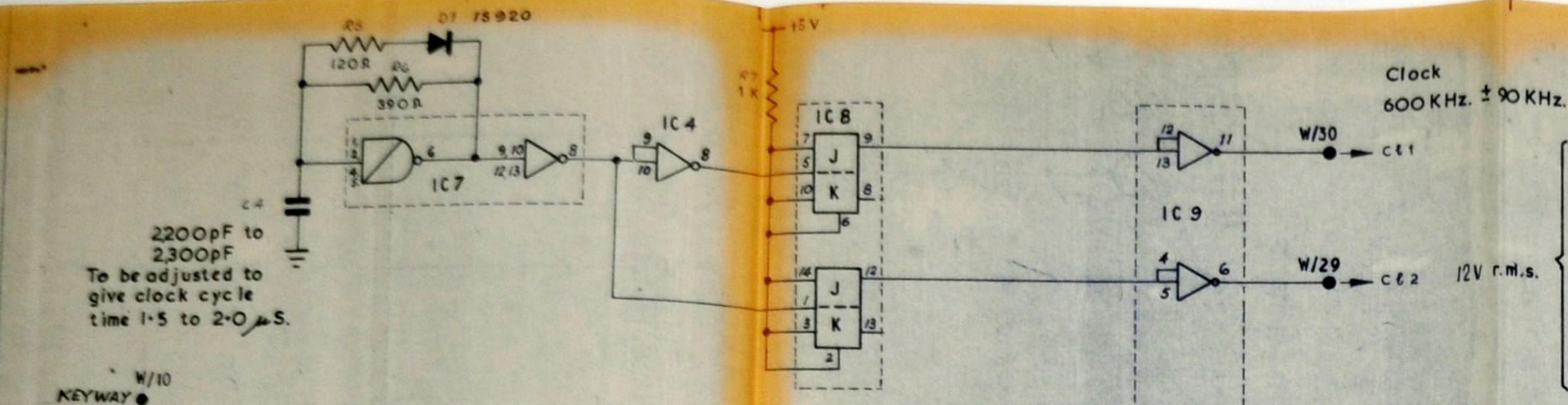
ALL RESISTORS ARE 1/4 W, 1%
UNLESS OTHERWISE STATED.

PC BOARD DWG 5B01261

SCHEDULE 5501236

TITLE			D.D.M. 2.	
DIGITAL TO ANALOGUE LOGIC DIAGRAM.			PCB223/1	
DWG No 6B01212			REF 1212	
ISSUE	DATE	SIGNATURE		
D.	15-11-72	Reason		
C	15-11-72	Reason		

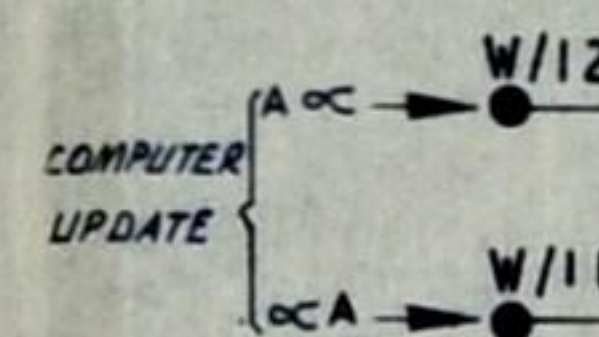
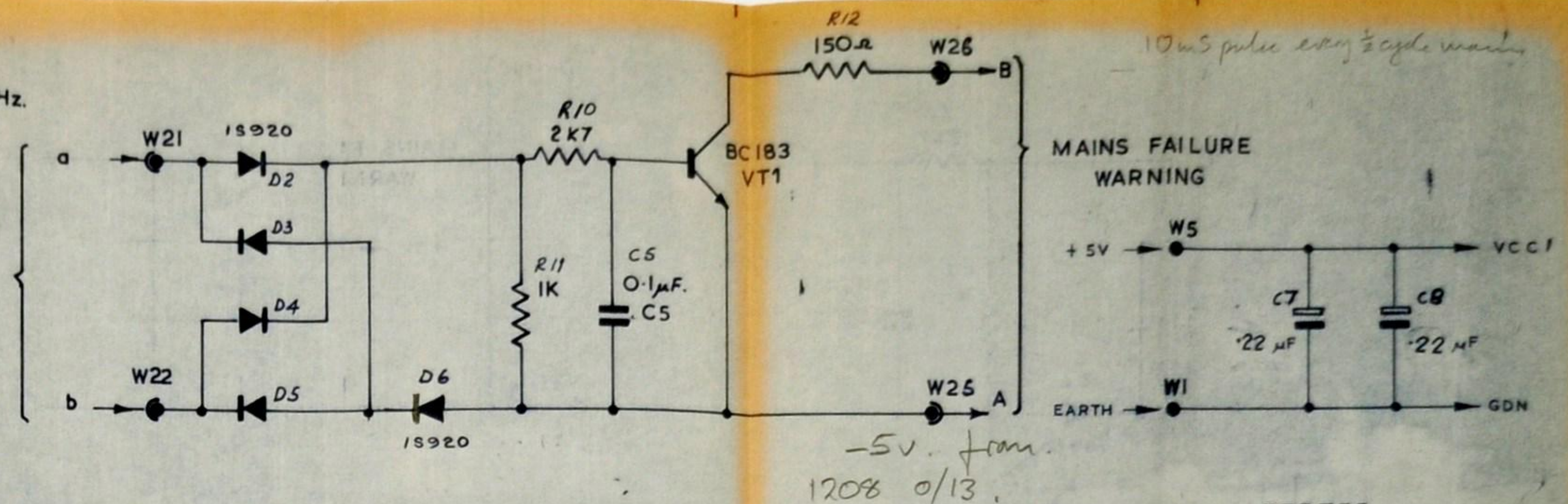




NOTE:- ALL RESISTORS ARE
1/4W $\pm$ 5% UNLESS OTHER-
WISE SPECIFIED.

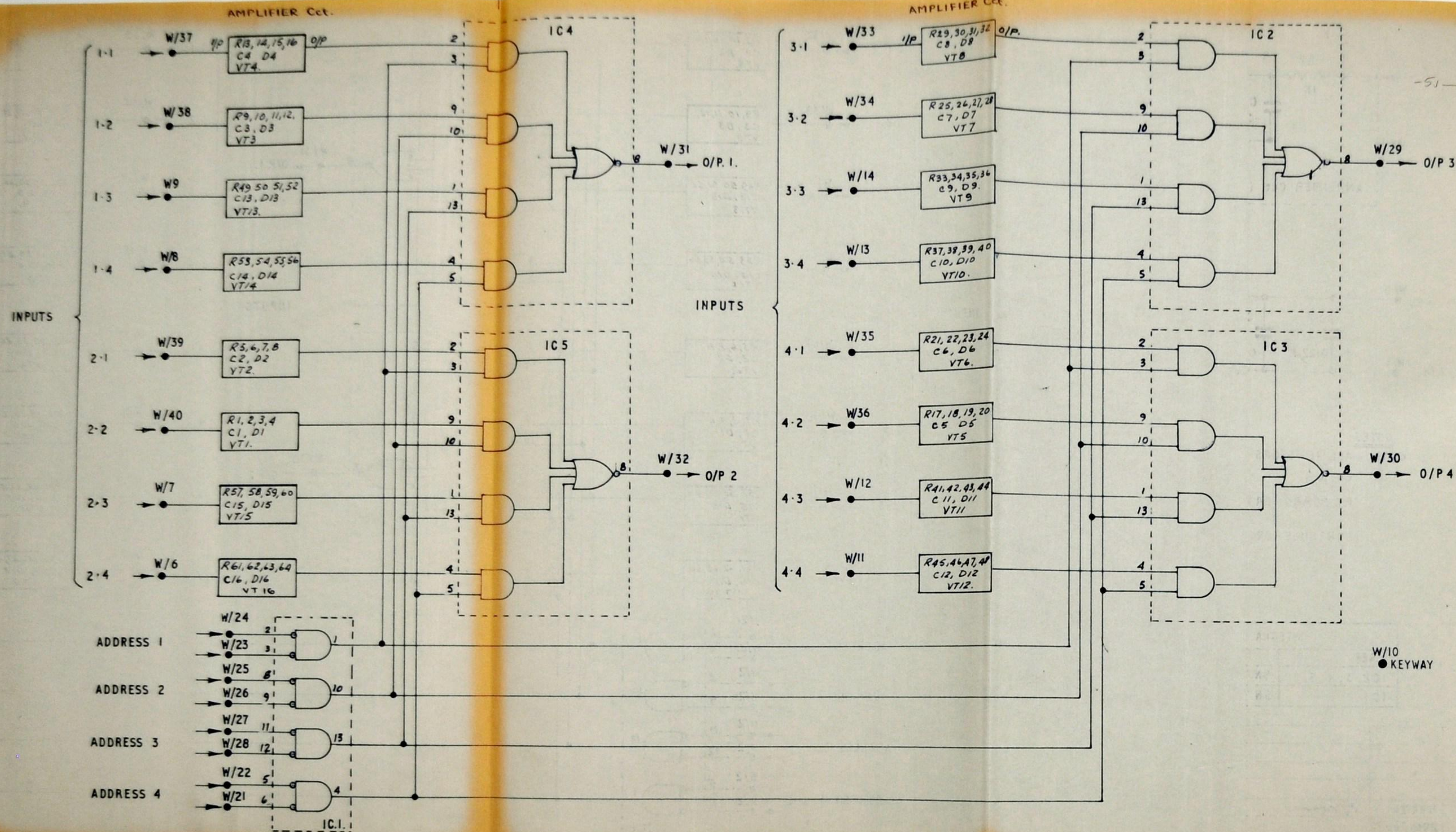
P.C. BOARD DRG. - 5B01263
SCHEDULE: - 5501238

INTEGRATED CIRCUITS			
REF NO.	TYPE	Vcc	GND
IC 11	SN74LO4N	PIN 14	PIN 7
IC 14	SN75451AP	PIN 8	PIN 4
IC 1, 2, 3, 13	SN74L122N	PIN 14	PIN 7
IC 4, 5, 12	SN74LOON	" 14	" 7
IC 6	SN7404N	" 14	" 7
IC 7	SN7413N	" 14	" 7
IC 8, 10	SN74L73N	" 4	" 11
IC 9	SN7437N	" 14	" 7

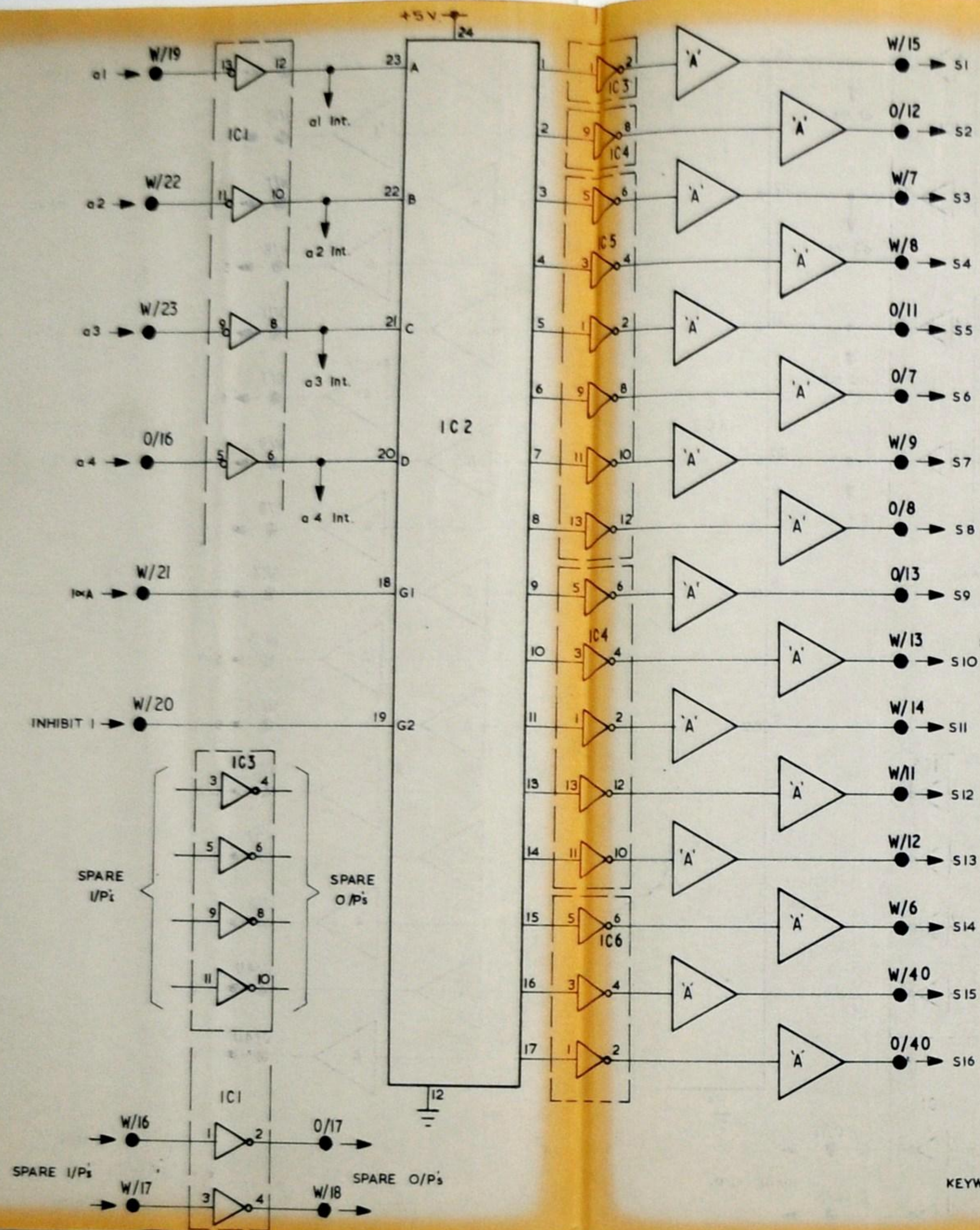


ISSUE	DATE	SIGNATURE
G.	8.12.72	R. Eason
F.	3.10.72	R. Eason
E.	12.9.72	R. Eason
D.	22.8.72	R. Eason
C.	27.4.72	R. Eason
B.	25.1.72	R. Eason
A.	29.12.71	R. Eason

TITLE	
DDM 2 CONTROL (GENERAL) LOGIC DIAGRAM.	
PCB 224	REF. 1213
DRG. NO. 6B01213	



			TITLE.	
			DDM 2	
			SWITCH INTERFACE	
			LOGIC DIAG.	
			REF. 1214	
C	11-2-72	R. Rasm	PC225	
B	29th Feb 72		DRG No. 6B01214	
ISSUE	DATE	SIGNATURE		

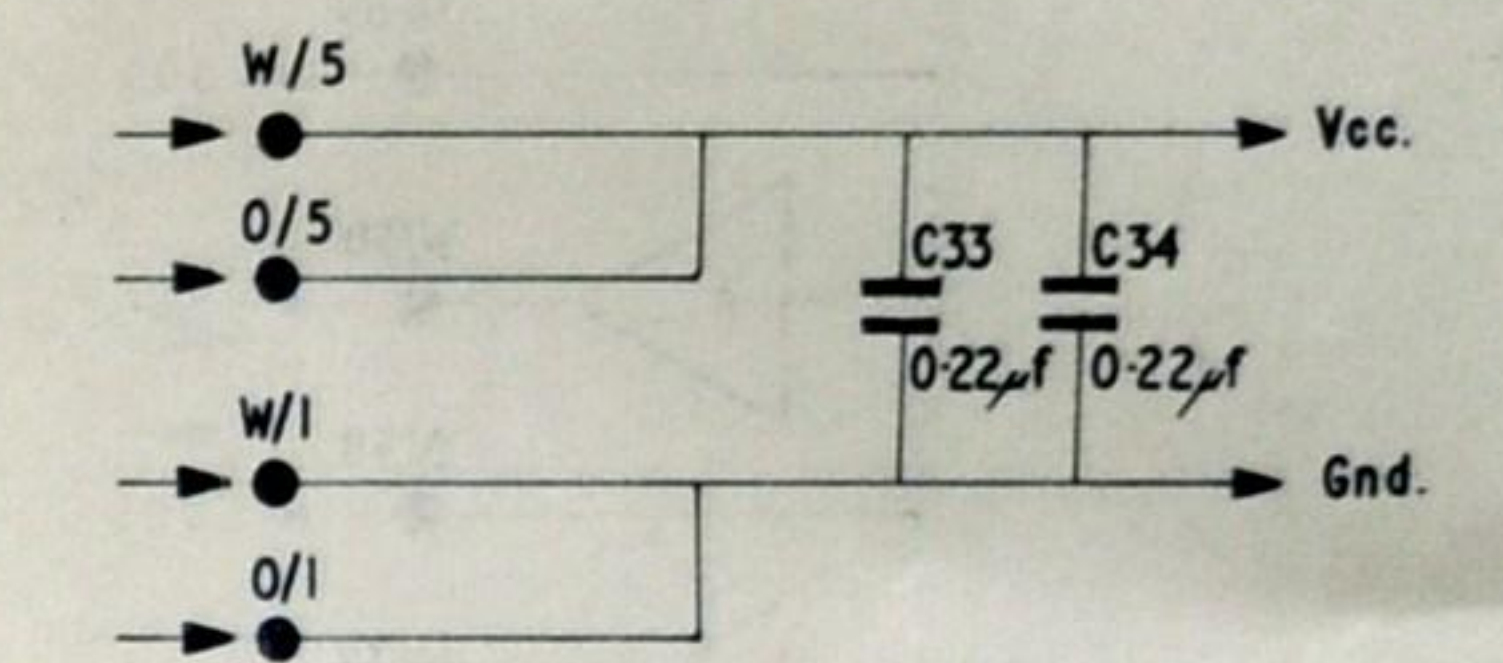
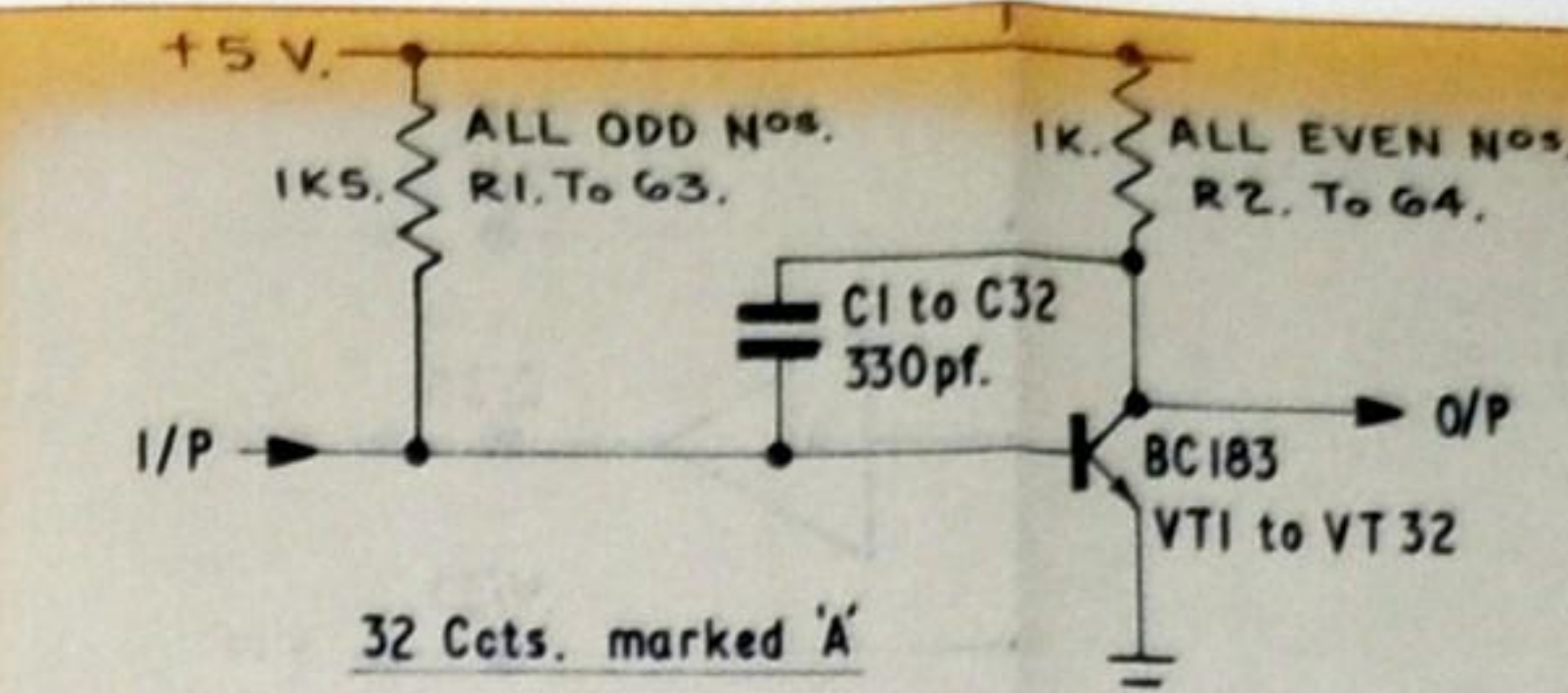
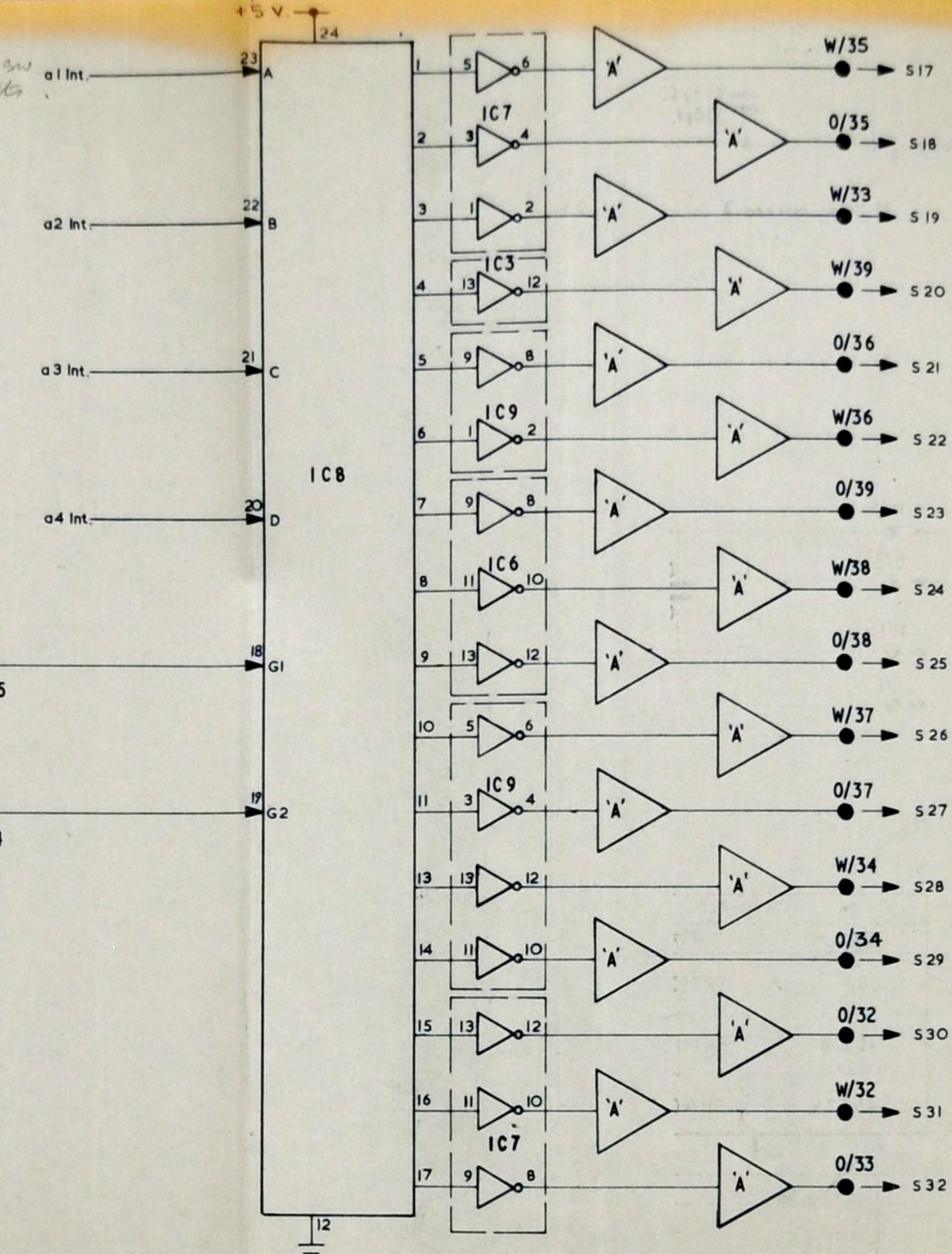


to 748 and
contacts

2 α A
W/25

INHIBIT 2
W/24

KEYWAY
● W/10
● O/10



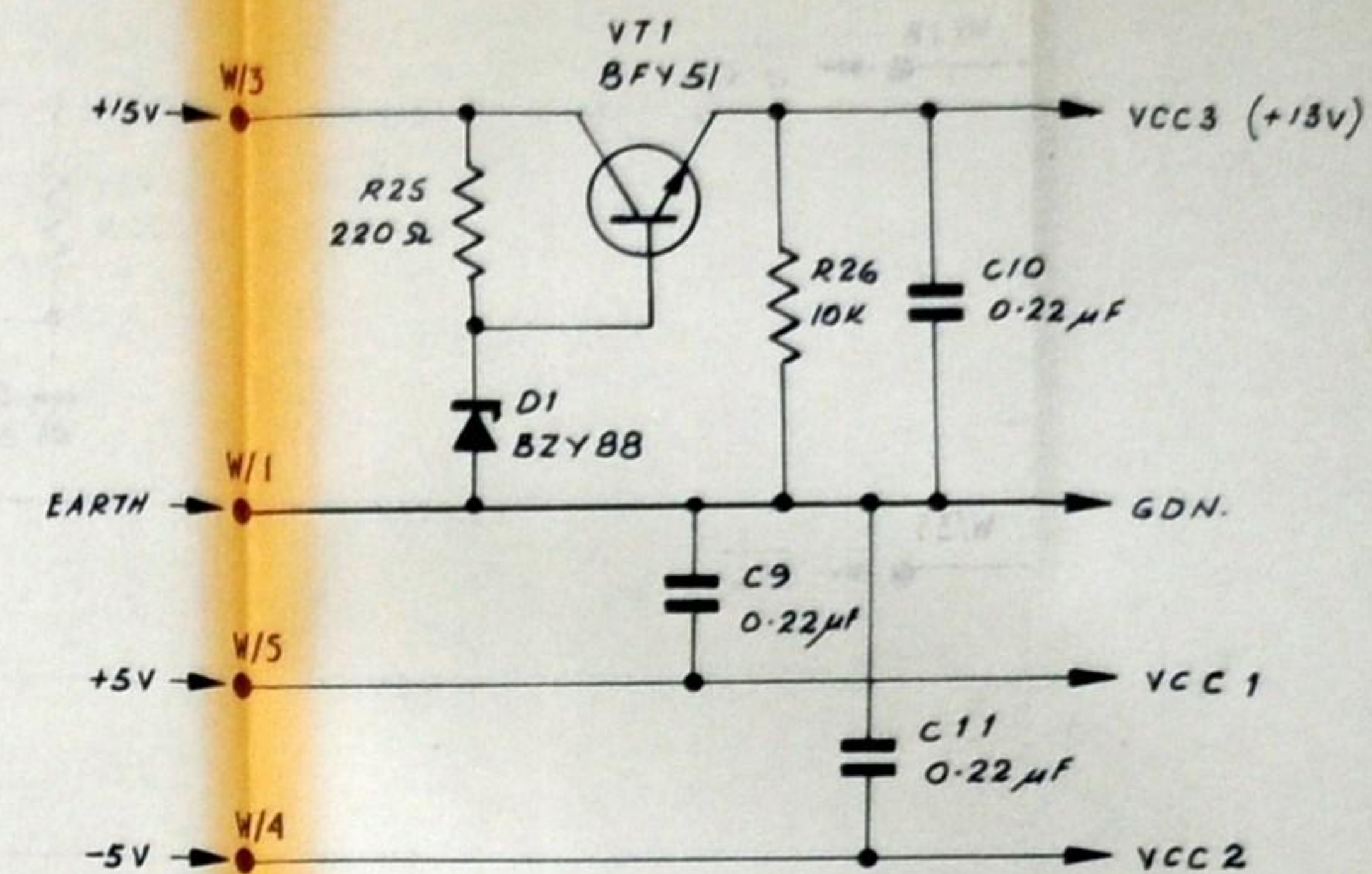
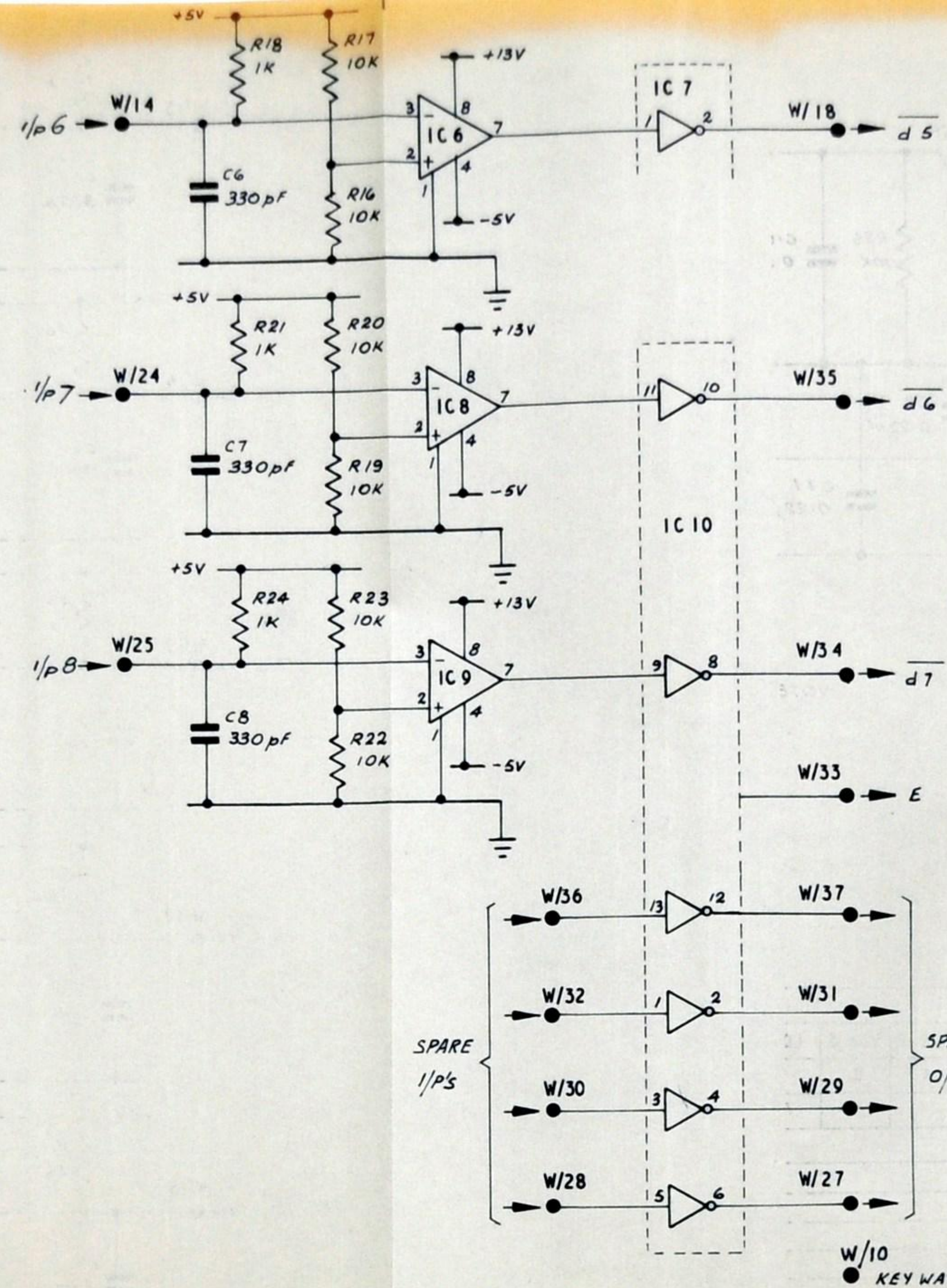
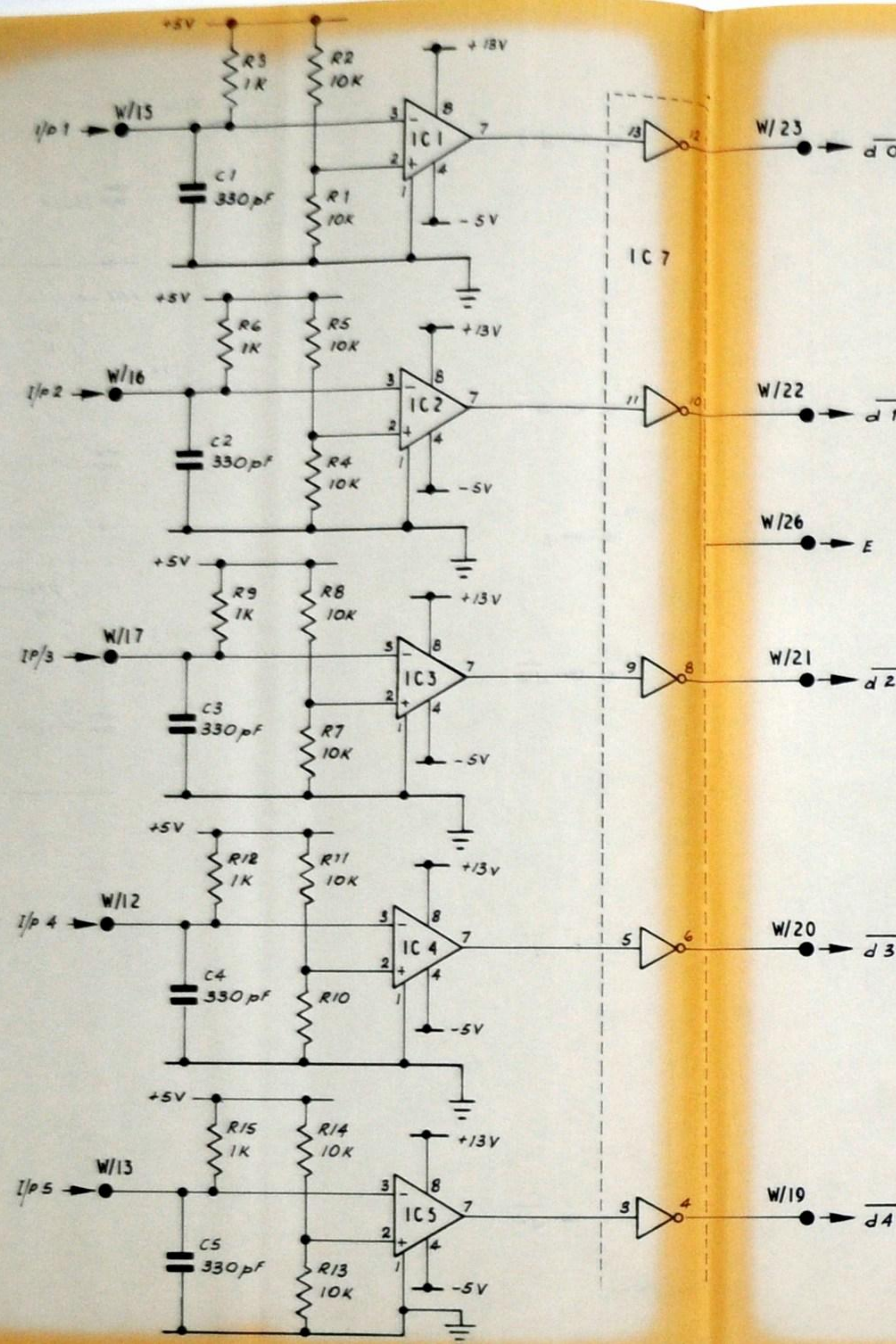
NOTES:

P.C. BOARD DRG. No. 5801265

SCHEDULE 5501240.

INTEGRATED CIRCUITS.			
REF. NO.	TYPE	VCC	GDN.
IC 1	SN7404N	Pin 14	Pin 7
IC 2, 8	SN74154N	Pin 24	Pin 12
IC 3, 4, 5, 6, 7, 9	SN7405N	Pin 14	Pin 7

TITLE			D.D.M. 2.	
CONTACT SCAN LOGIC			PCB 226	
REF. 1215			6801215	
ISSUE	DATE	SIGNATURE		
B	22-9-72			
A	10-5-72			



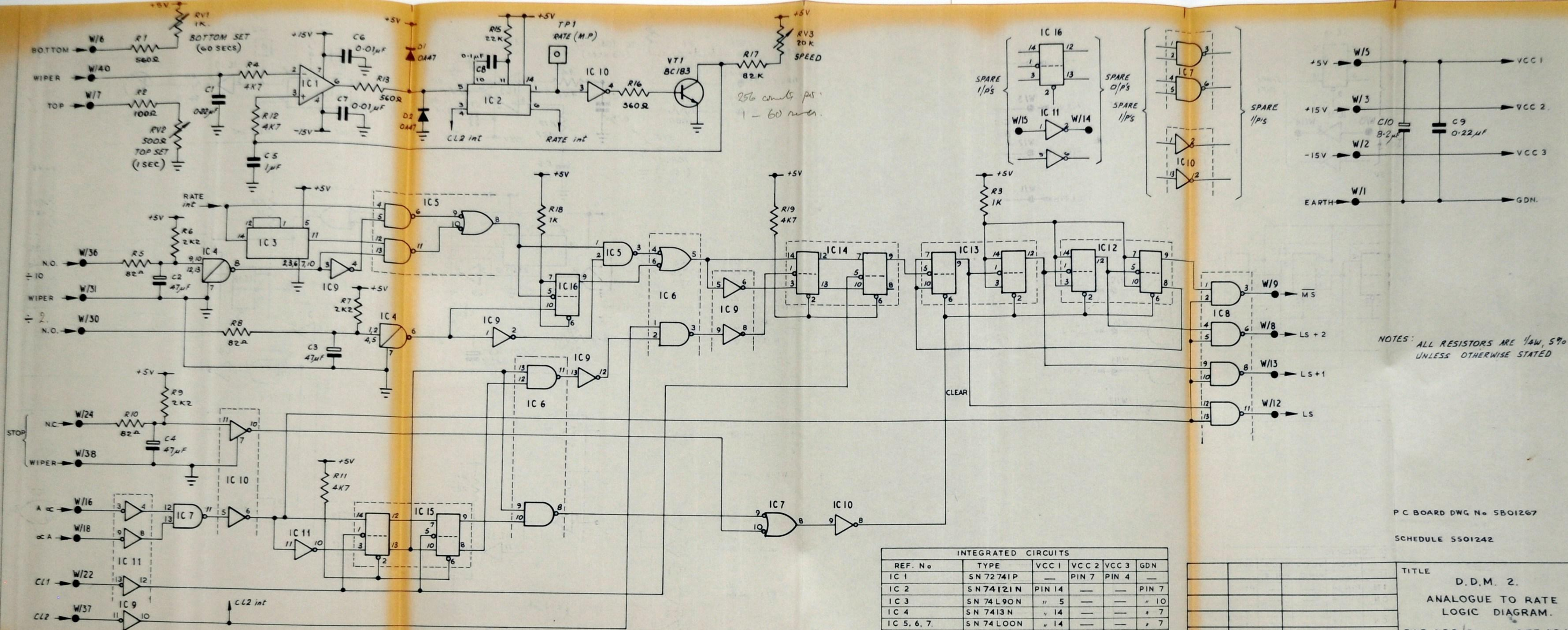
NOTES:
ALL RESISTORS ARE 1/4W, 5%
UNLESS OTHERWISE STATED

INTEGRATED CIRCUIT					
REF. N°	TYPE	Vcc 1	Vcc 2	Vcc 3	GDN
IC 1,2,3,4,5,6,8,9	SN 72810 P		4	8	
IC 7,10	SN 74L04N	14			7

PC BOARD DWG No 5801266.

SCHEDULE 5501241.

TITLE:-			
D.D.M. 2.			
SCAN RECEIVERS			
LOGIC DIAGRAM			
C	1.6.73	R. Eason	PC227
B	4.12.72	R. Eason	REF 1216
ISSUE	DATE	SIGNATURE	DWG. No 6B01216

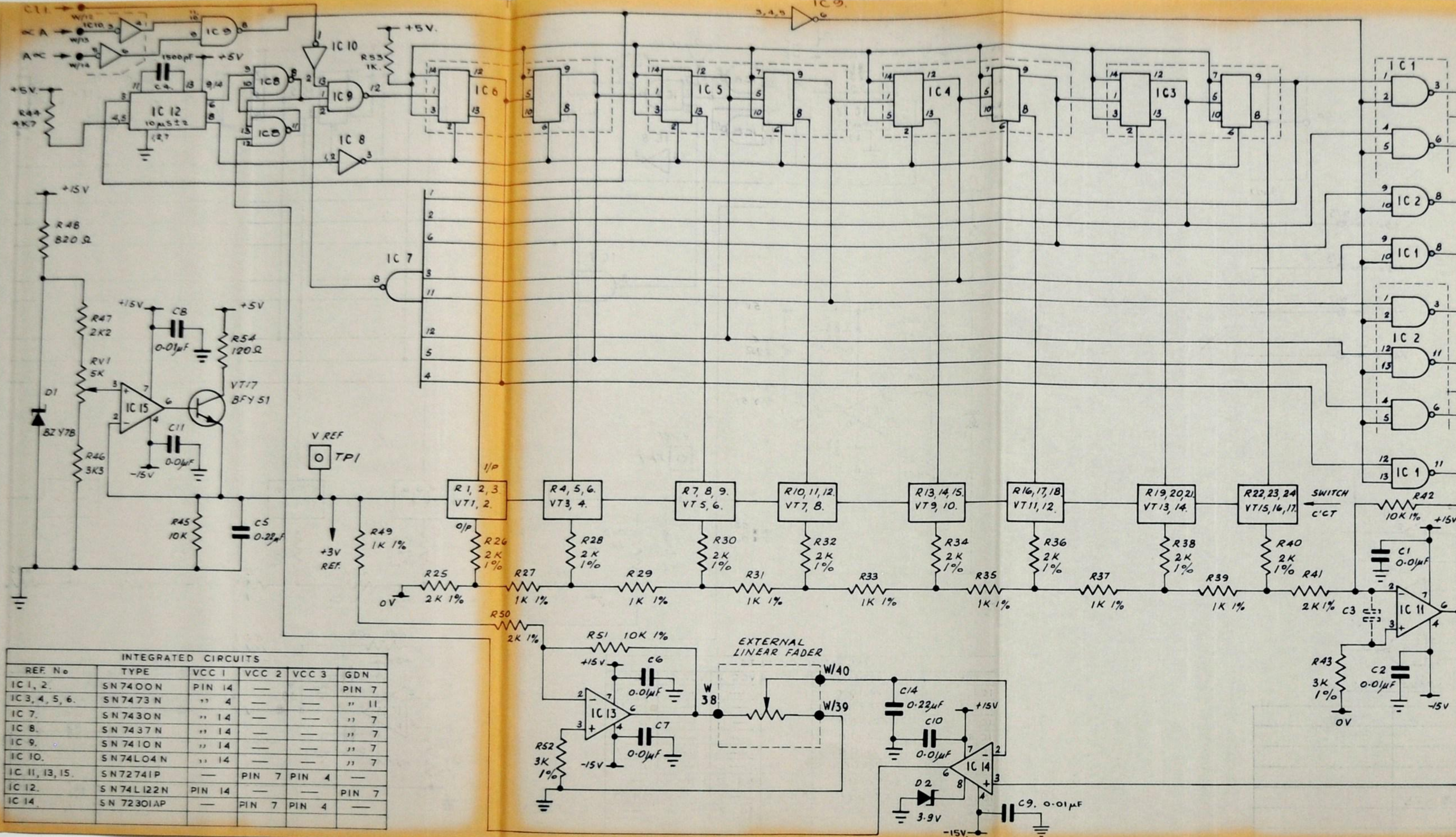


PC BOARD DWG No 5B01267

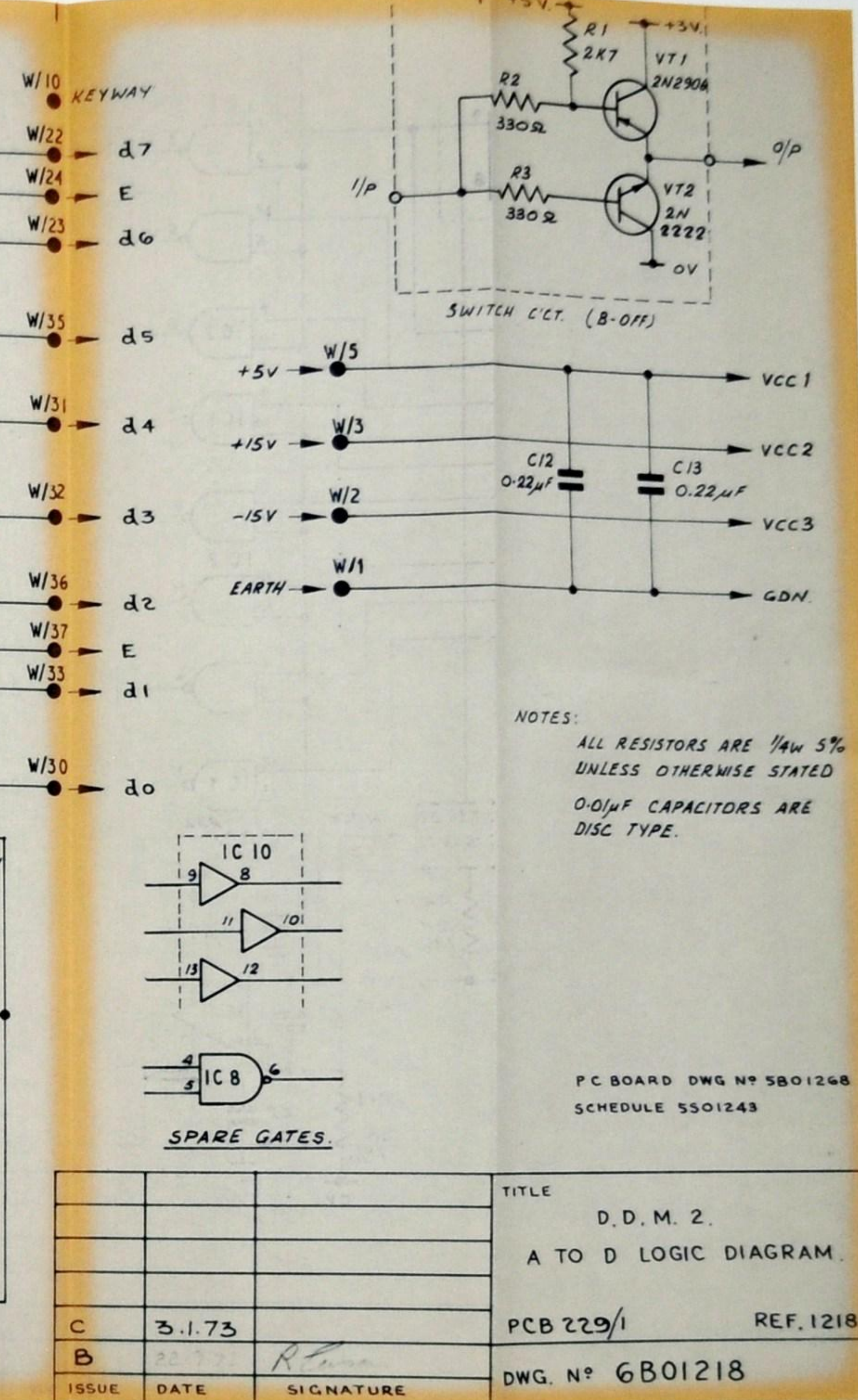
SCHEDULE 5501242

INTEGRATED CIRCUITS					
REF. No	TYPE	VCC 1	VCC 2	VCC 3	GDN
IC 1	SN 72741P	—	PIN 7	PIN 4	—
IC 2	SN 74121N	PIN 14	—	—	PIN 7
IC 3	SN 74L90N	" 5	—	—	" 10
IC 4	SN 7413N	" 14	—	—	" 7
IC 5, 6, 7	SN 74LOON	" 14	—	—	" 7
IC 8	SN 7400N	" 14	—	—	" 7
IC 9, 11	SN 74LO4N	" 14	—	—	" 7
IC 10	SN 7404N	" 14	—	—	" 7
IC 12, 13, 14, 15, 16	SN 74L73N	" 4	—	—	" 11

			TITLE D.D.M. 2. ANALOGUE TO RATE LOGIC DIAGRAM. PCB 228/2 REF. 1217
D	20.9.72	R. P. S.	DWG No 6B01217
ISSUE	DATE	SIGNATURE	



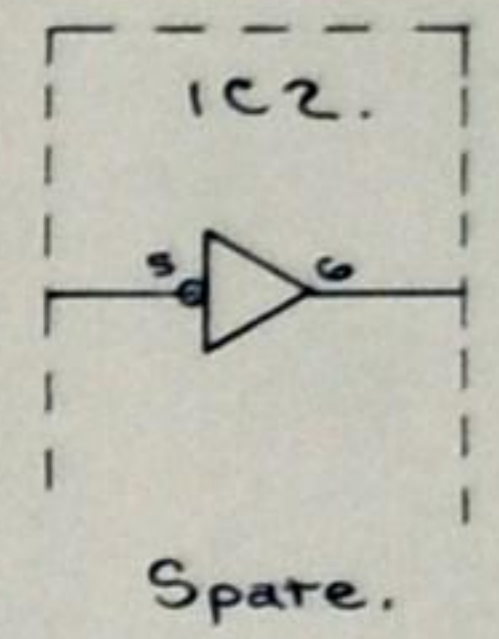
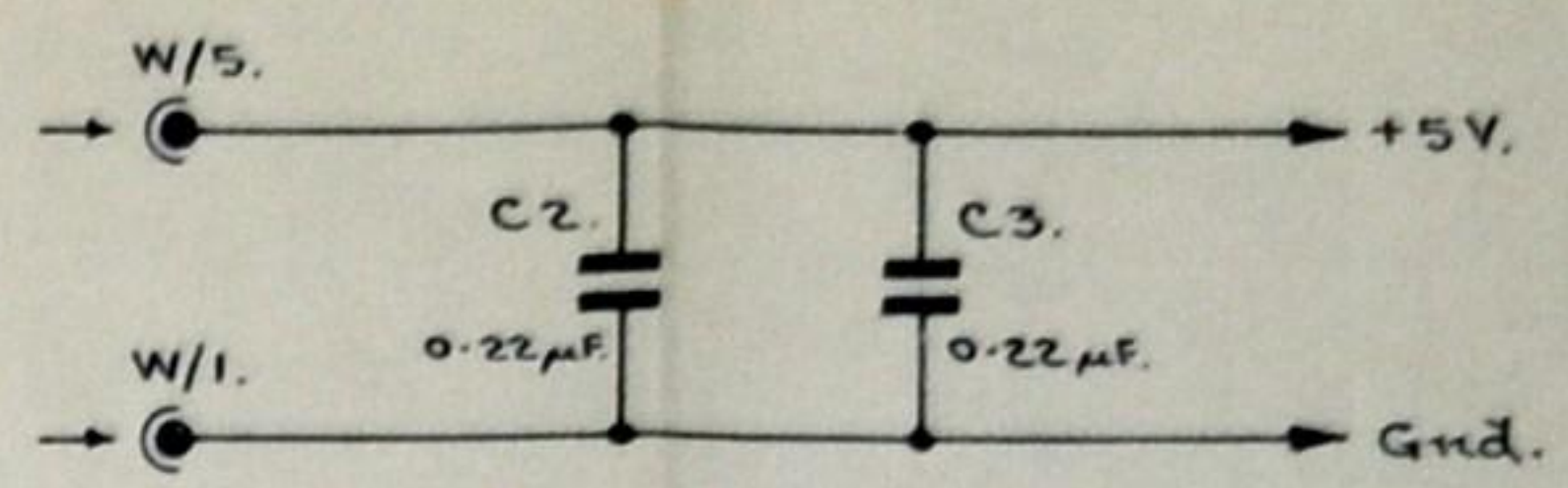
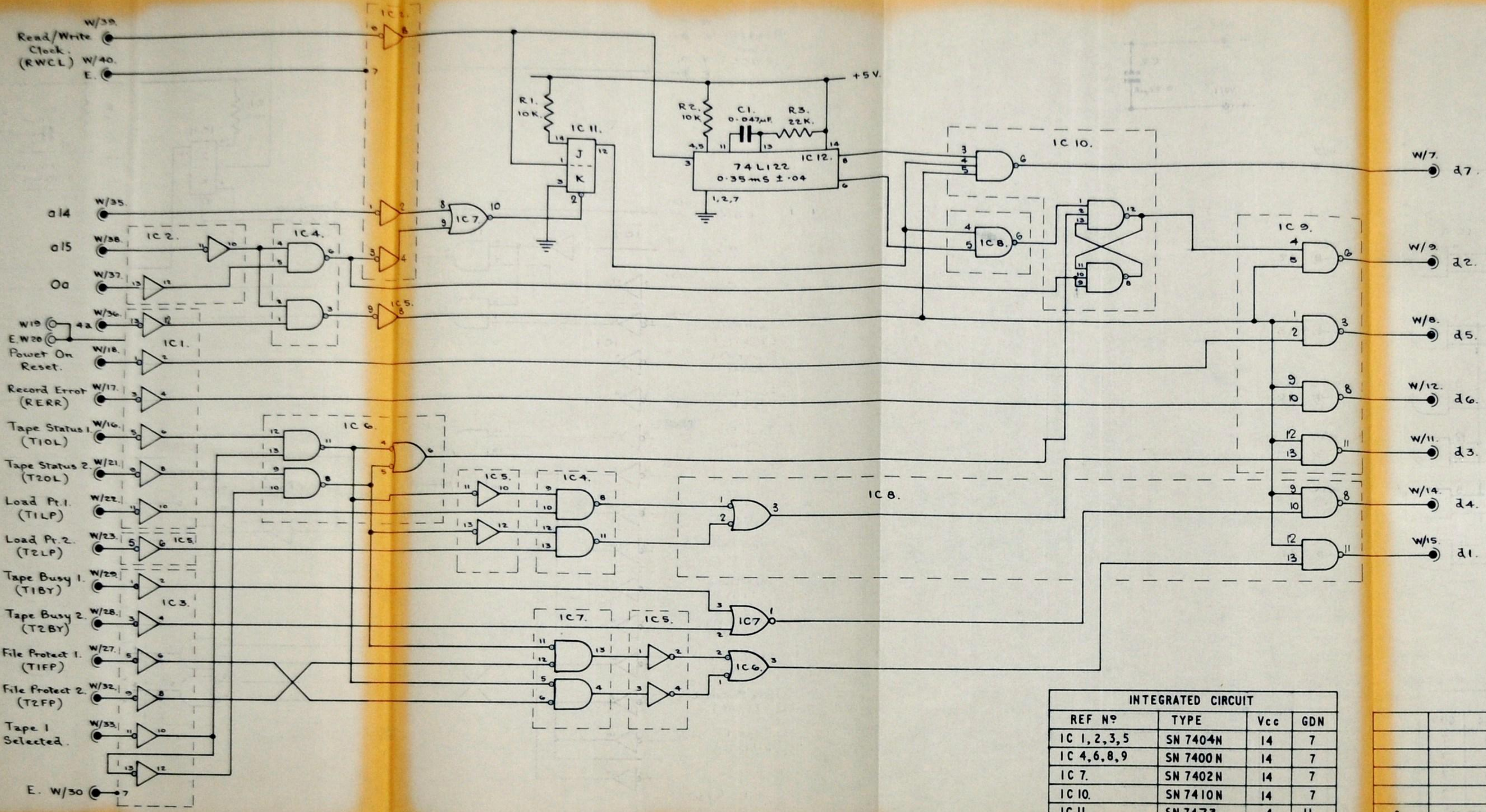
INTEGRATED CIRCUITS					
REF No	TYPE	VCC 1	VCC 2	VCC 3	GDN
IC 1, 2	SN7400N	PIN 14	—	—	PIN 7
IC 3, 4, 5, 6	SN7473N	" 4	—	—	" 11
IC 7	SN7430N	" 14	—	—	" 7
IC 8	SN7437N	" 14	—	—	" 7
IC 9	SN7410N	" 14	—	—	" 7
IC 10	SN74LO4N	" 14	—	—	" 7
IC 11, 13, 15	SN72741P	—	PIN 7	PIN 4	—
IC 12	SN74L122N	PIN 14	—	—	PIN 7
IC 14	SN72301AP	—	PIN 7	PIN 4	—



NOTES:
ALL RESISTORS ARE 1/4W 5%
UNLESS OTHERWISE STATED
0.01μF CAPACITORS ARE
DISC TYPE.

PC BOARD DWG NO 5801268
SCHEDULE 5501243

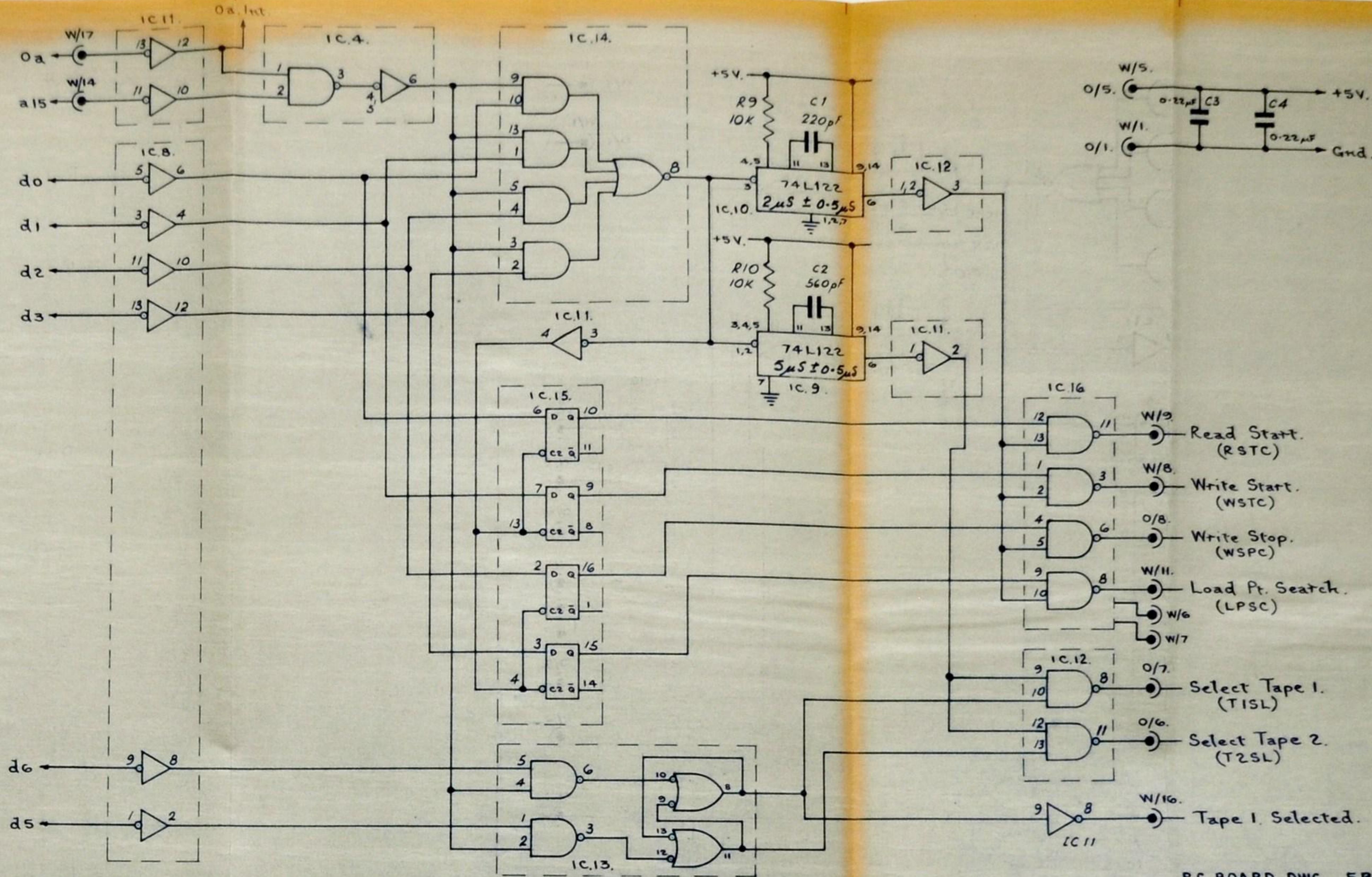
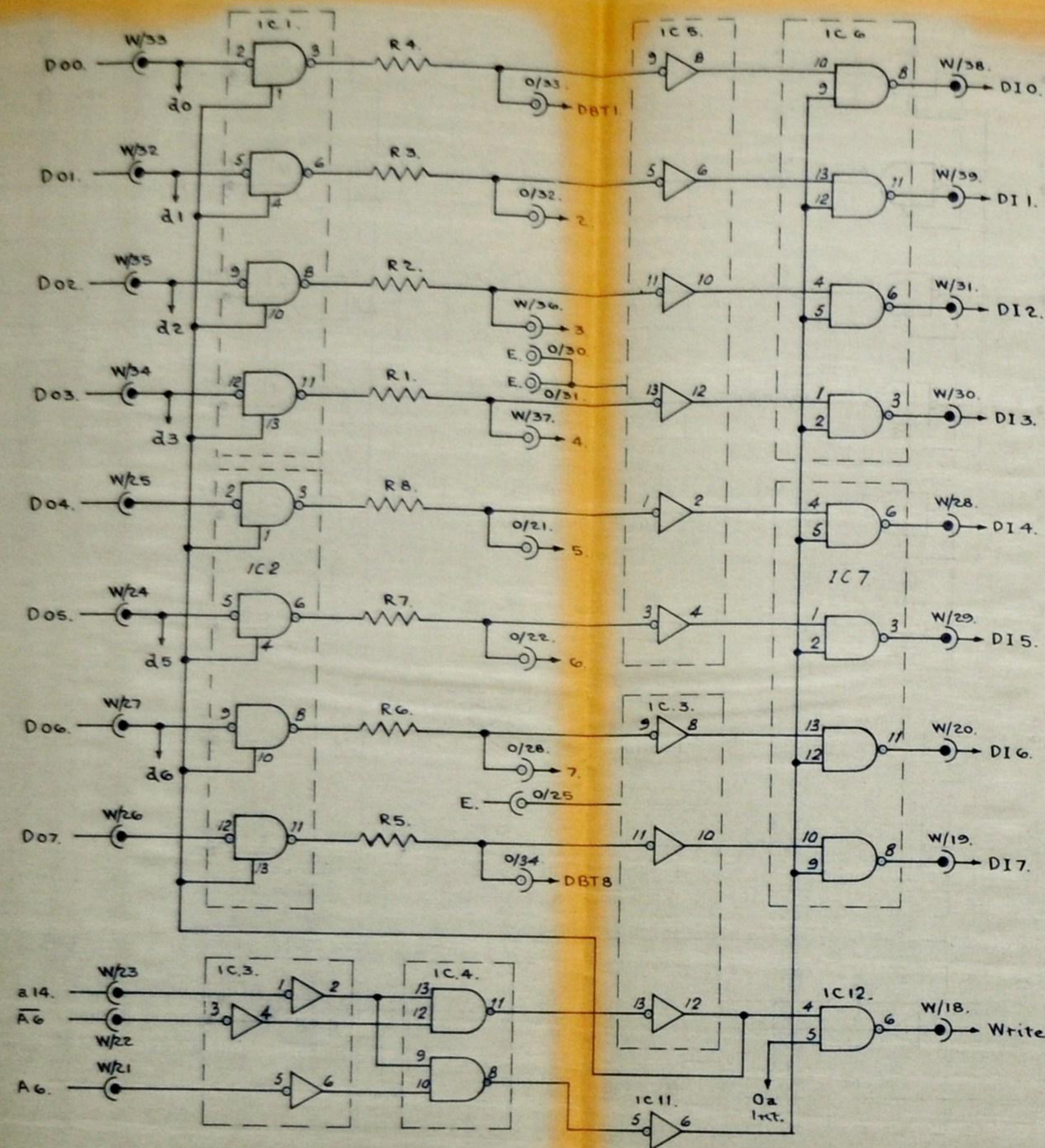
TITLE			D.D.M. 2.	
A TO D LOGIC DIAGRAM.			REF. 1218	
PCB 229/1			REF. 1218	
DWG. NO 6B01218			REF. 1218	
ISSUE	DATE	SIGNATURE		
C	3.1.73			
B				



PC BOARD DWG. 5B01271.
SCHEDULE. 5S01246.

INTEGRATED CIRCUIT			
REF N°	TYPE	Vcc	GDN
IC 1,2,3,5	SN 7404N	14	7
IC 4,6,8,9	SN 7400N	14	7
IC 7.	SN 7402N	14	7
IC 10.	SN 7410N	14	7
IC 11.	SN 7473	4	11
IC 12.	SN 74L122N	14	7

			TITLE :- DDM 2 TAPE UNIT INTERFACE A STATUS.(CARTRIFILE 20) PCB232 REF.1223
A	11/10/73	R. Gagan	
ISSUE	DATE	SIGNATURE	DWG N° 6B01223



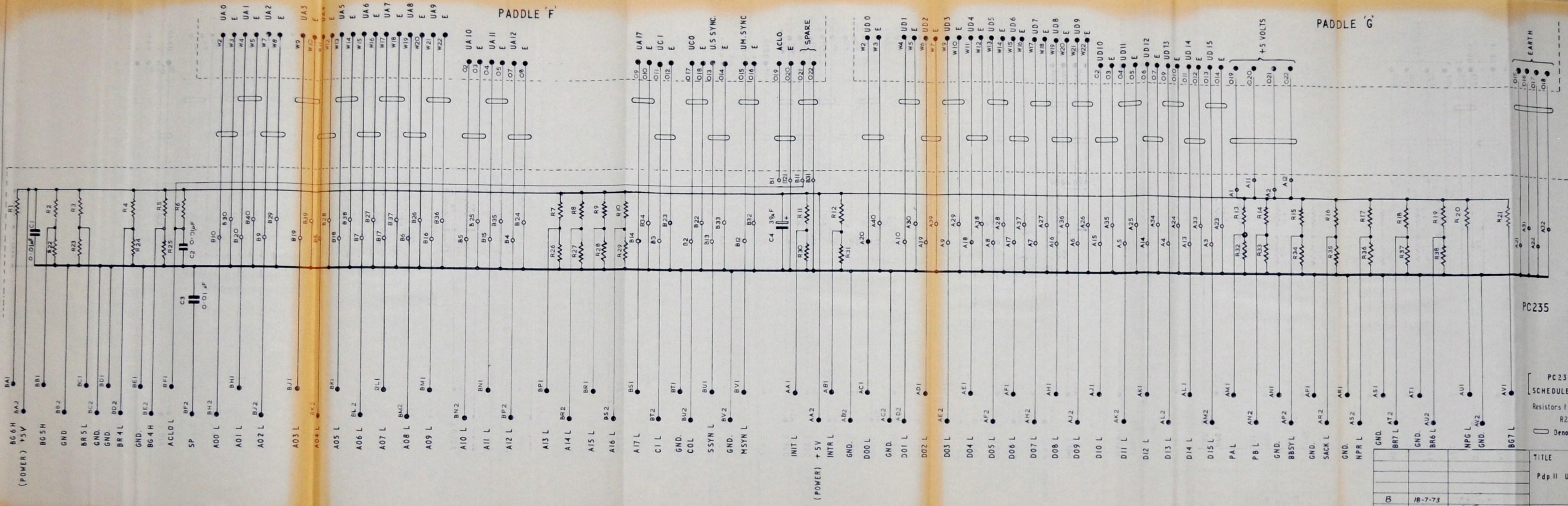
R1-8, 68Ω

INTEGRATED CIRCUIT			
REF. No	TYPE	VCC	GDN
ICB	SN 7404	PIN 14	PIN 7

INTEGRATED CIRCUIT			
REF No	TYPE	Vcc	GDN
IC 1,2	DM 8094	14	7
IC 3,5,11	SN 7404N	14	7
IC 4,6,7,12,13,16	SN 7400N	14	7
IC 14	SN 7454N	14	7
IC 15	SN 74175N	5	12
IC 9,10	SN 74L122N	14	7

TITLE:-			DDM
TAPE UNIT INTERFACE B			CONTROL & DATA
CARTRIFILE 20			PCB233
PCB233			REF.1224
DWG. No. 6B01224			
A	4-10-72	Reason	
ISSUE	DATE	SIGNATURE	

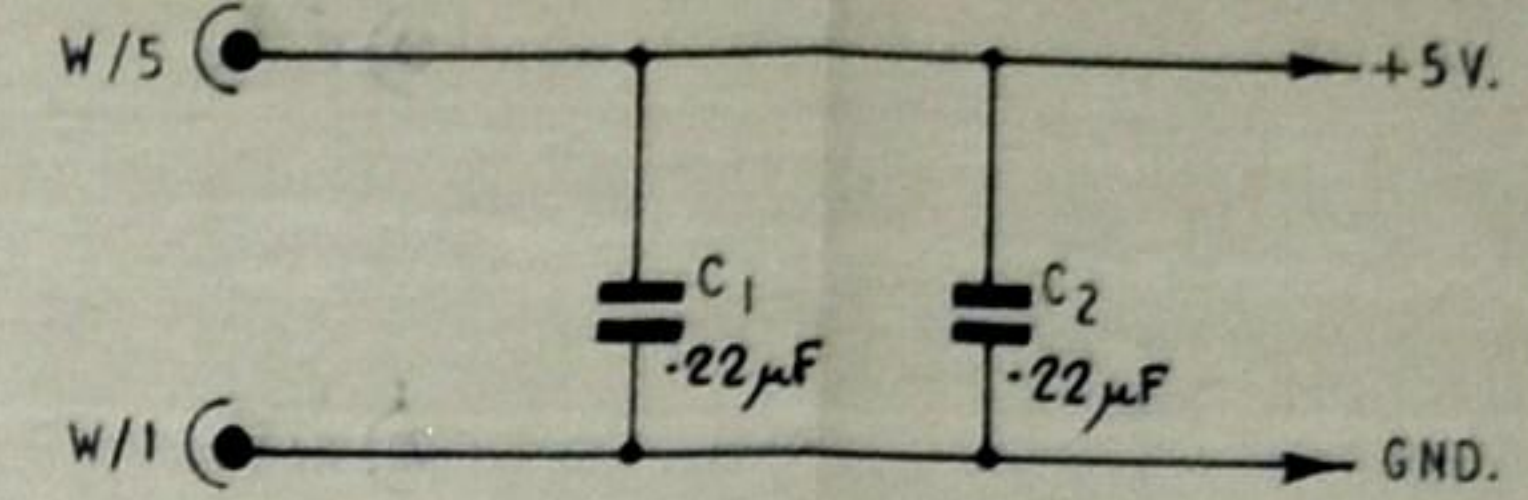
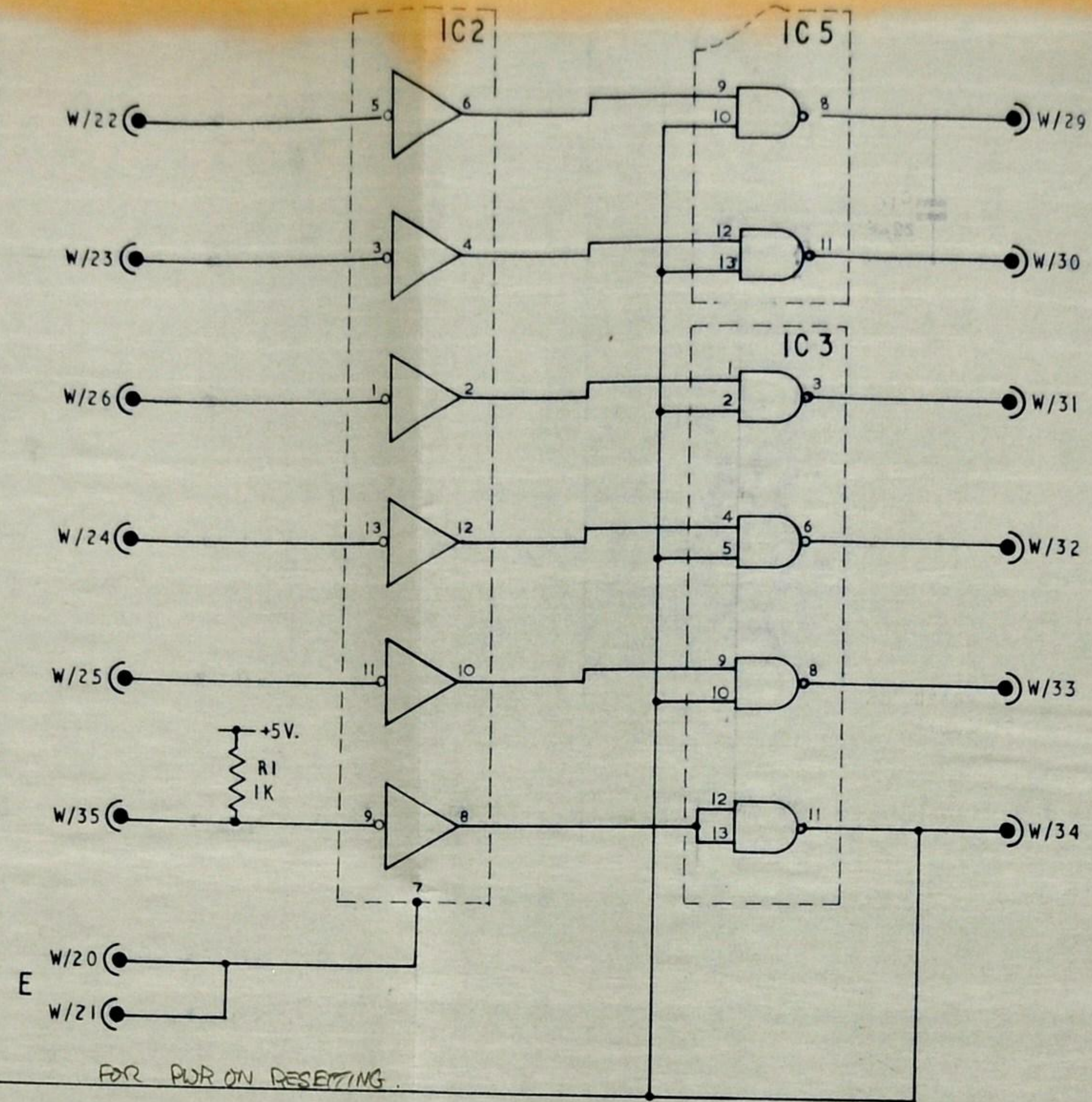
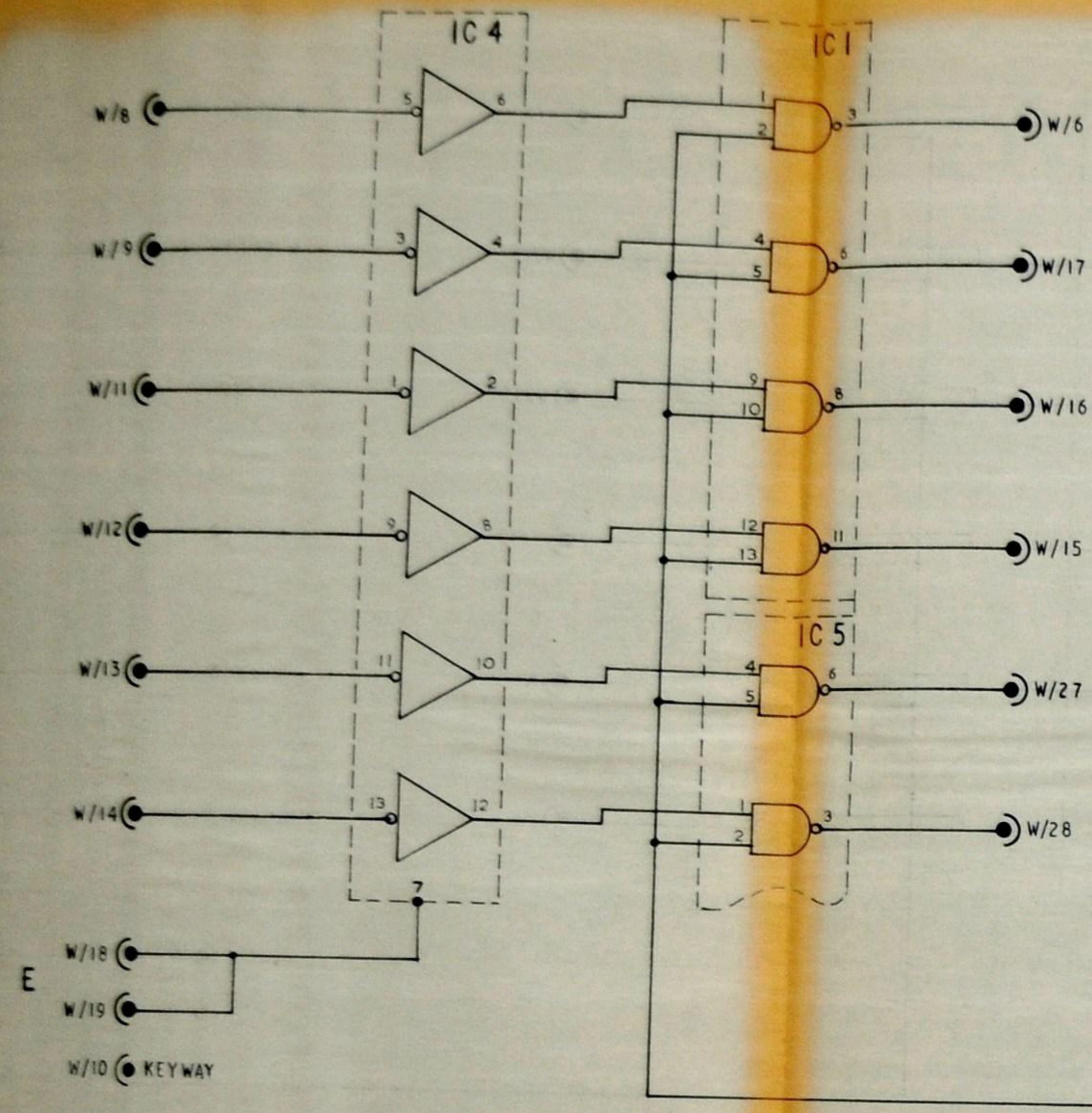
PC BOARD DWG. 5B01272
SCHEDULE 5S01247



PC235 REF1226
[SCHEDULE No. 55 01248]
Resistors 1 to R21 are 180 ohms.
R22 to R38 are 390 ohms
Denotes twisted Pairs

TITLE		
Pdp 11 UNIBUS CONNECTOR		
B	18-7-73	RC
A	16-2-73	
ISSUE	DATE	SIGNATURE

6A01226

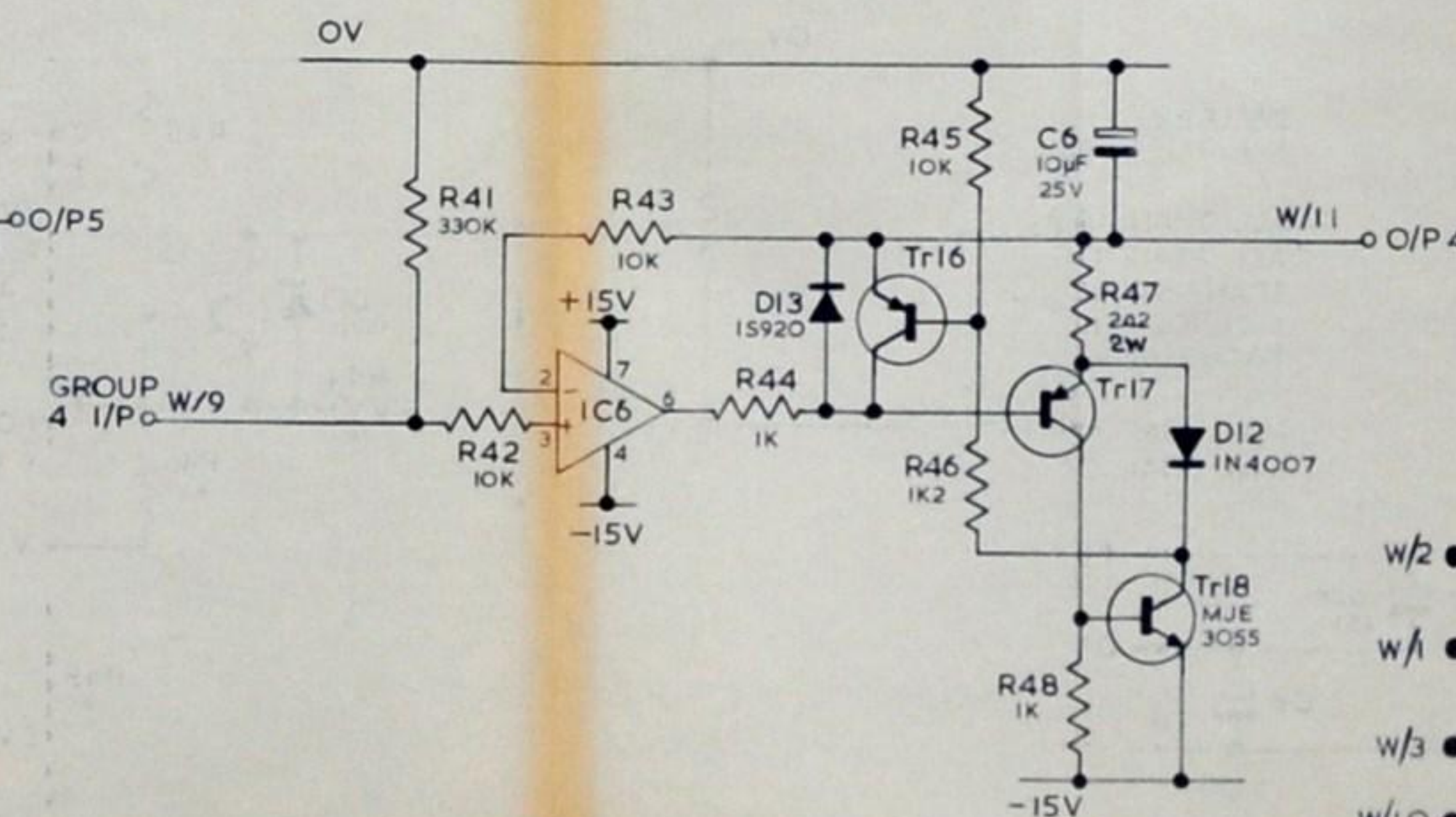
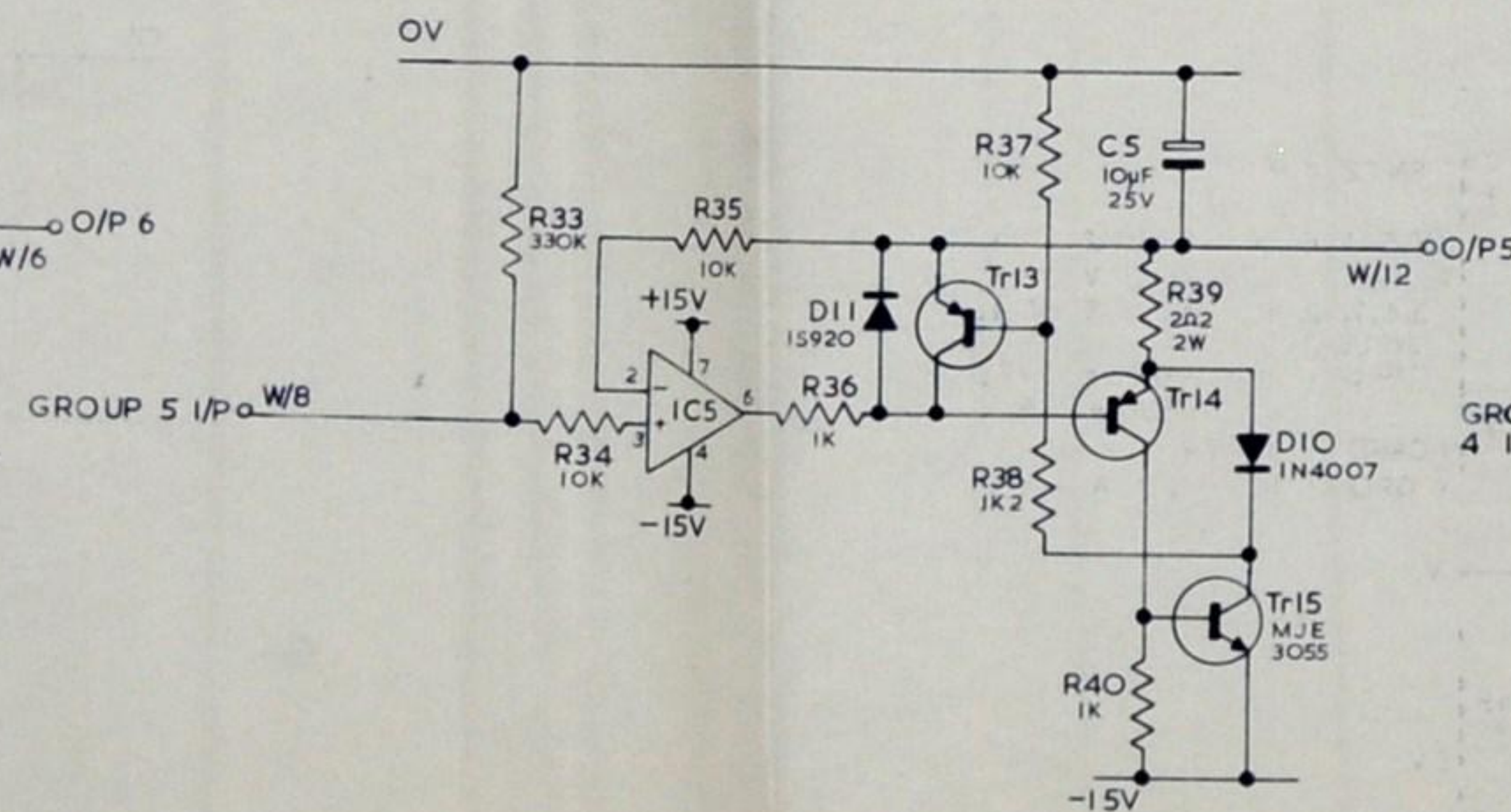
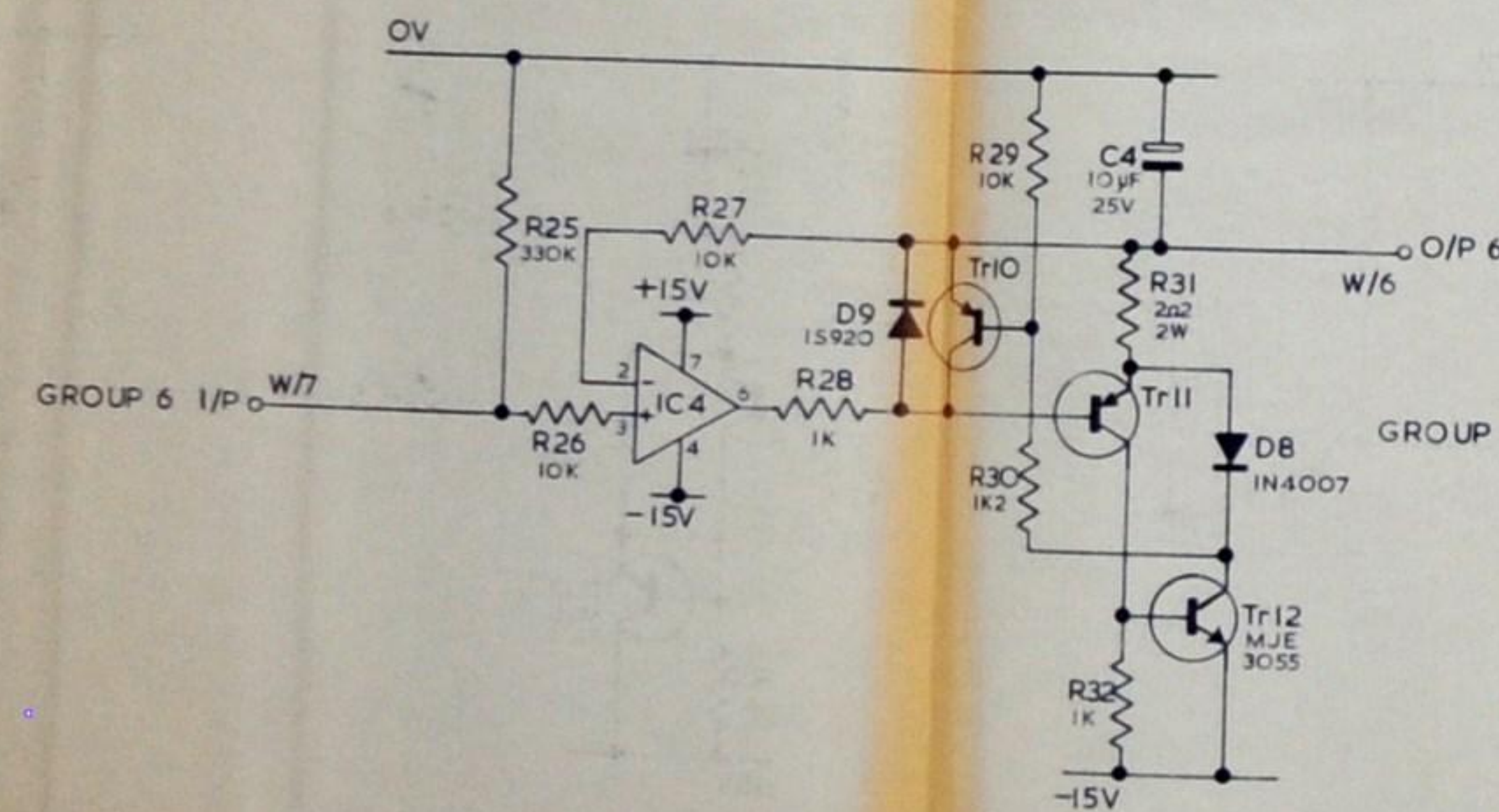
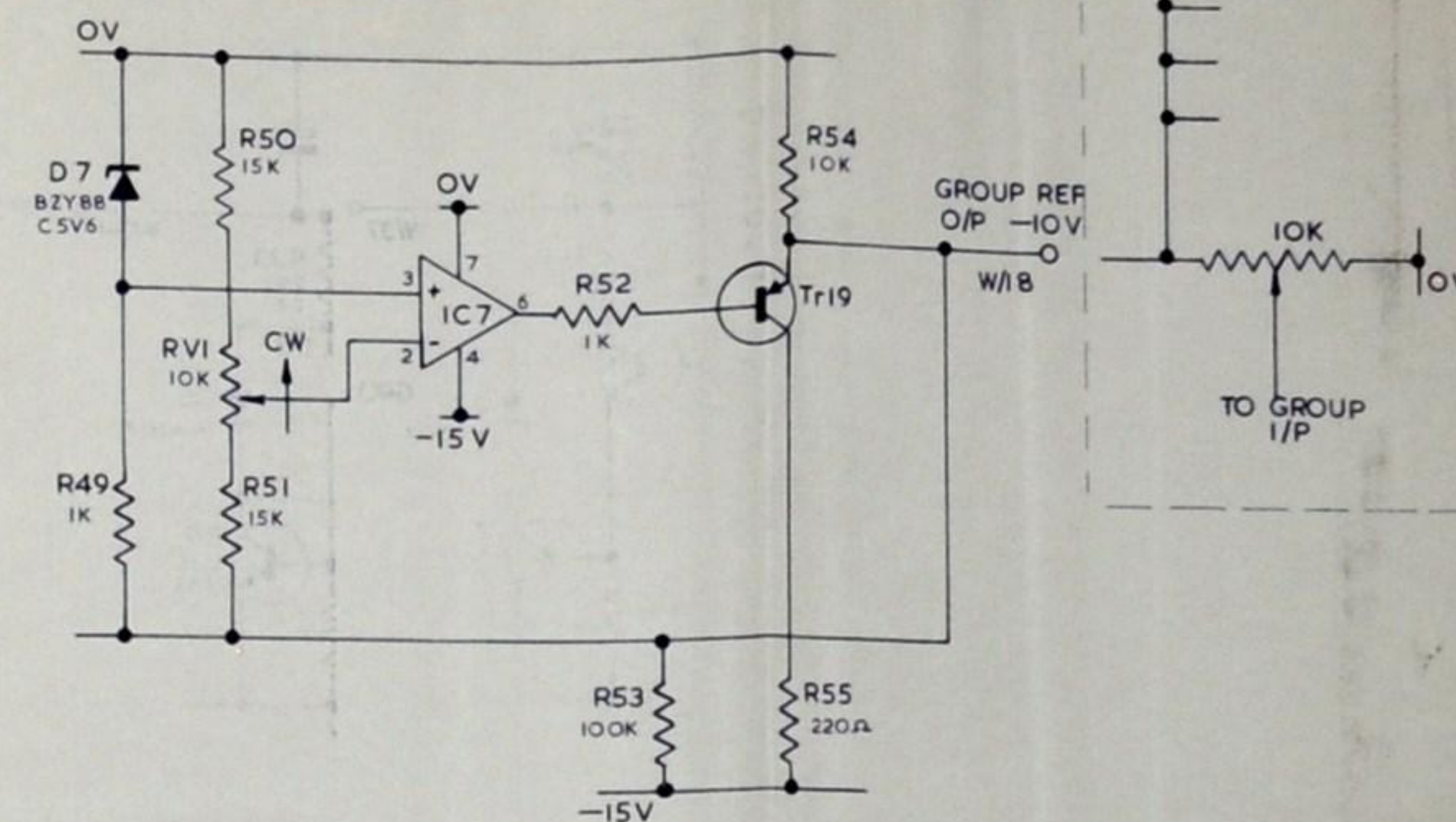
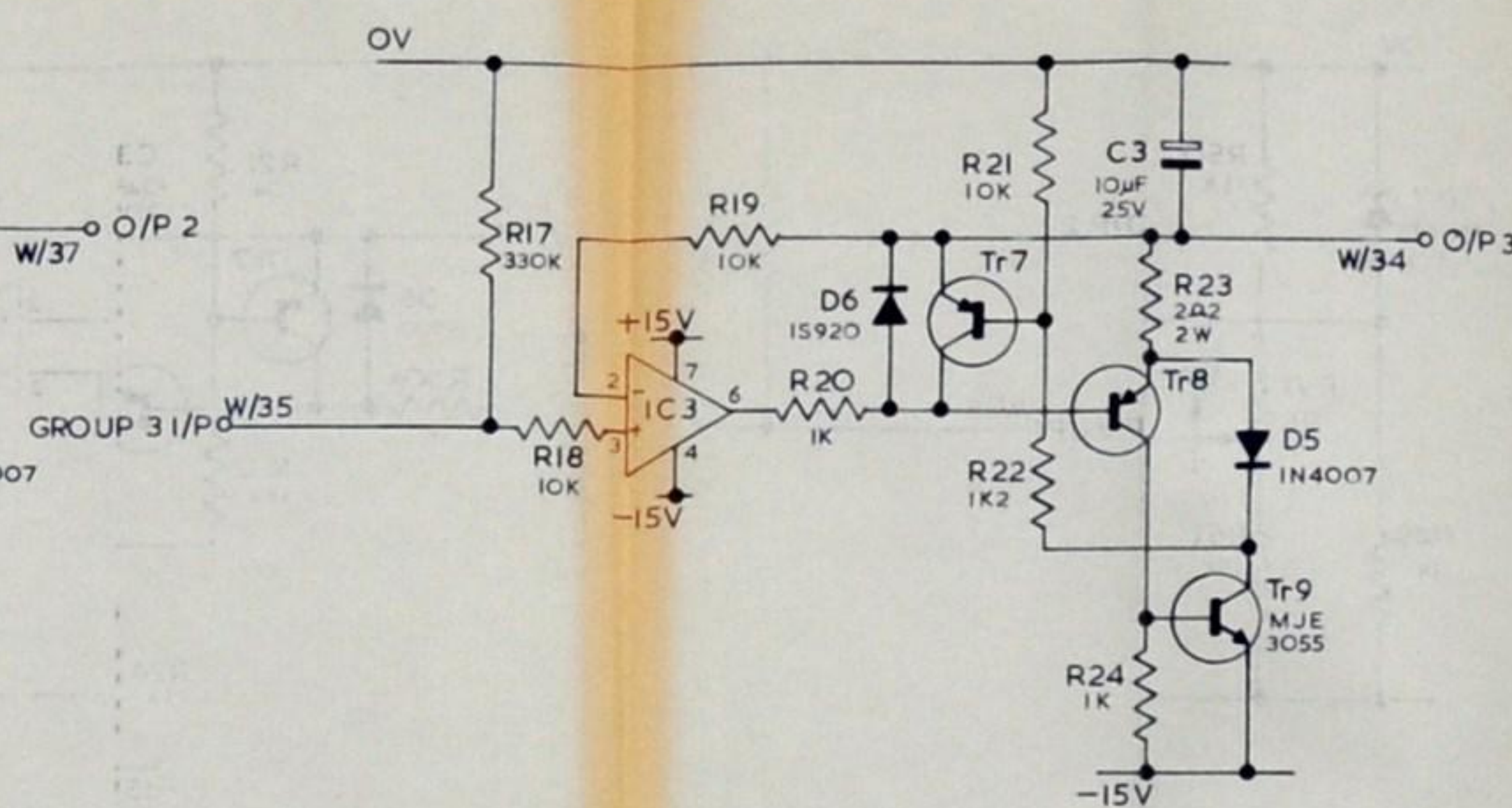
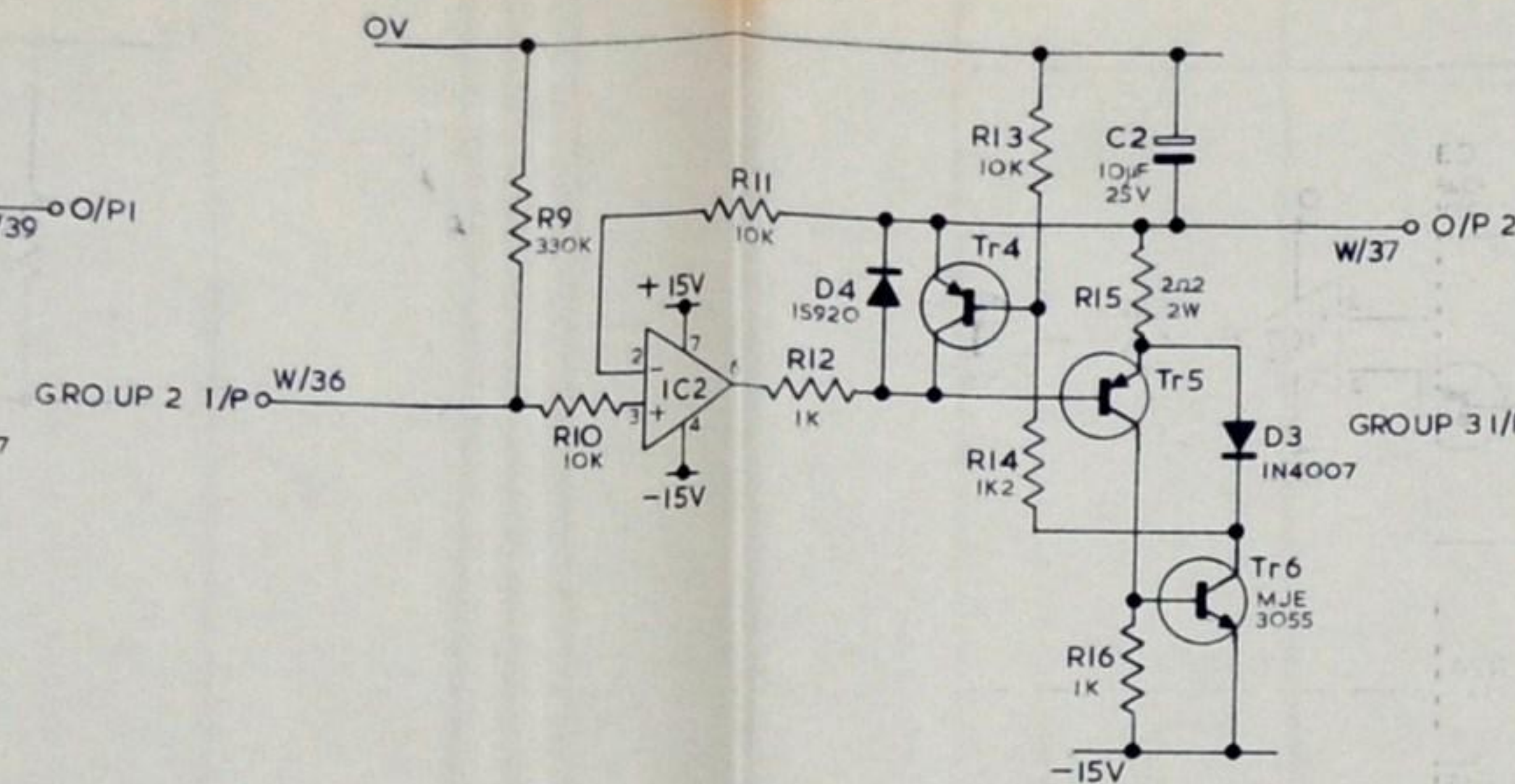
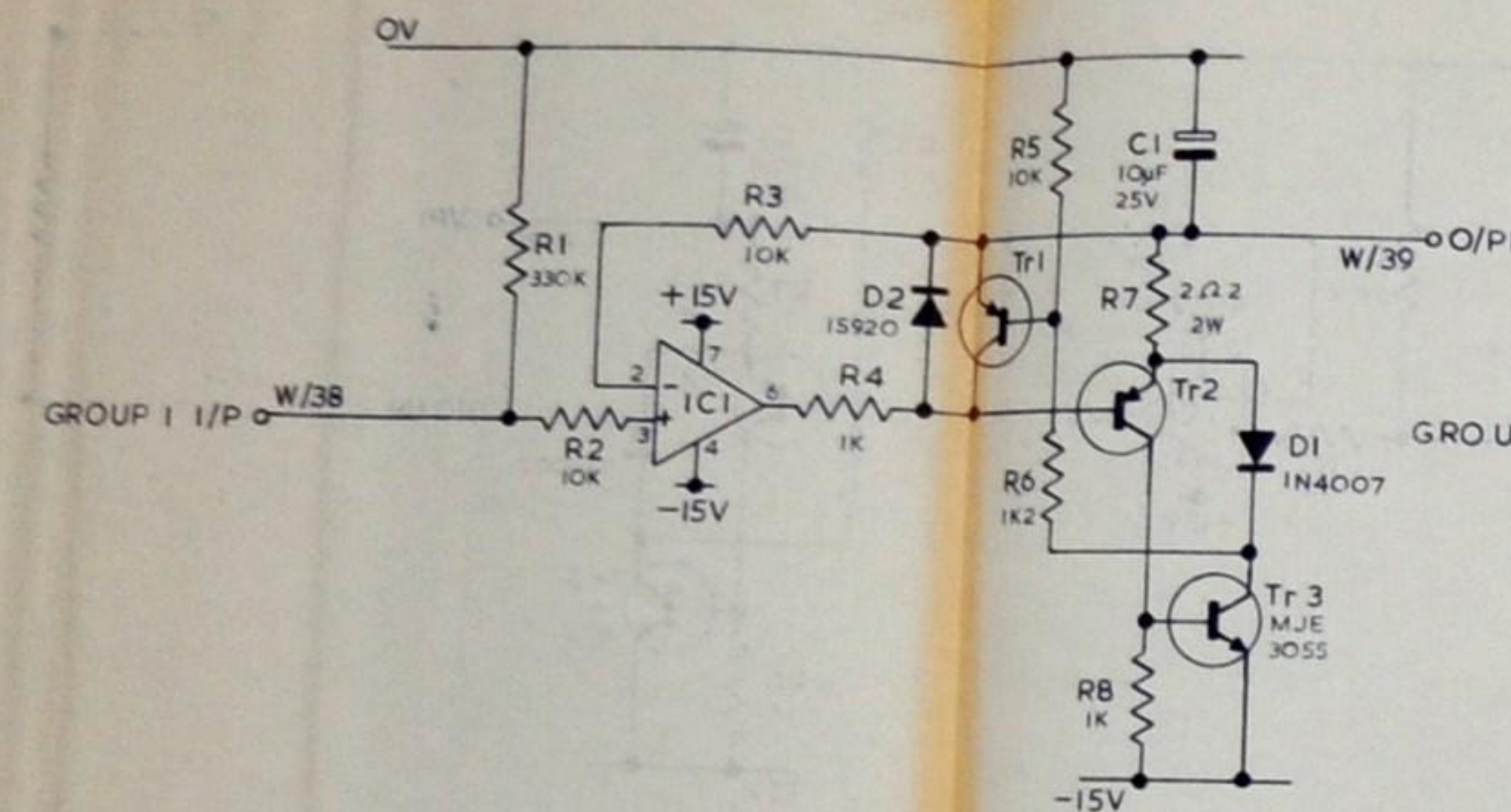


P.C. BOARD DRG.: 5B01278
SCHEDULE: 5501279

INTEGRATED CIRCUITS			
REF NO.	TYPE	+Vcc	GND.
IC 4, 2,	SN 7404N	14	7
IC 1, 3, 5,	SN 7437N	14	7

ISSUE	DATE	SIGNATURE
C	15.9.72	
B	12.9.72	
A	1.9.72	

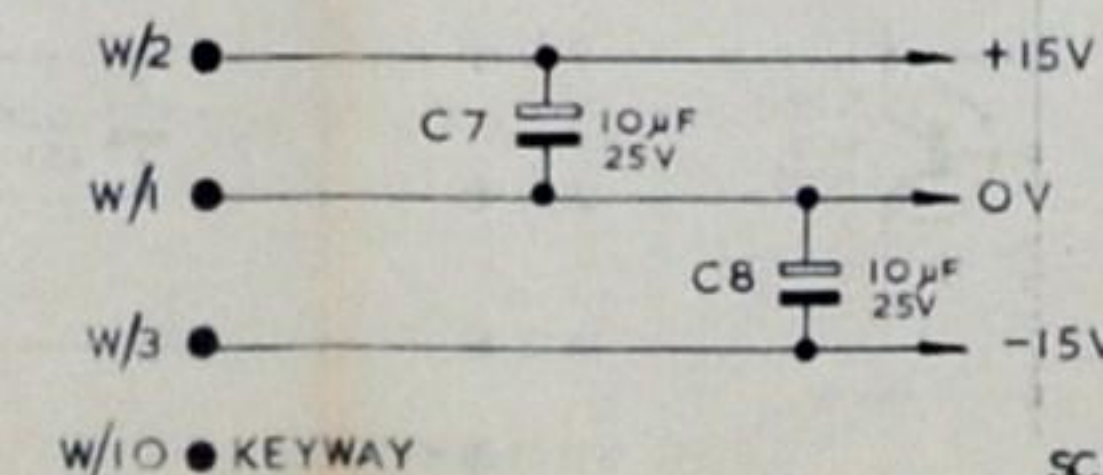
TITLE
DDM 2 BUFFER CARD
PCB 253/1 REF 1230
DRG. No. 6B01230



NOTES:-

ALL I.C's ARE SN72741P

ALL TRANSISTORS ARE BC 214 UNLESS OTHERWISE SPECIFIED.
ALL RESISTORS ARE CARBON 1/4W ± 5% UNLESS OTHERWISE SPECIFIED.
TRANSISTORS 3,6,9,12,15,18 MOUNTED ON A COMMON HEATSINK AND INDIVIDUALLY INSULATED.
EACH GROUP O/P CAN GIVE > 400mA @ -10V O/P
< 100mA @ 5/c - OV
MAX. LOAD ON CARD - 400mA
MAX. LOAD ON GROUP REF. - 20mA @ -10V



SCHEDULE:- 5501245
PCB 268 DRG:- 5501269

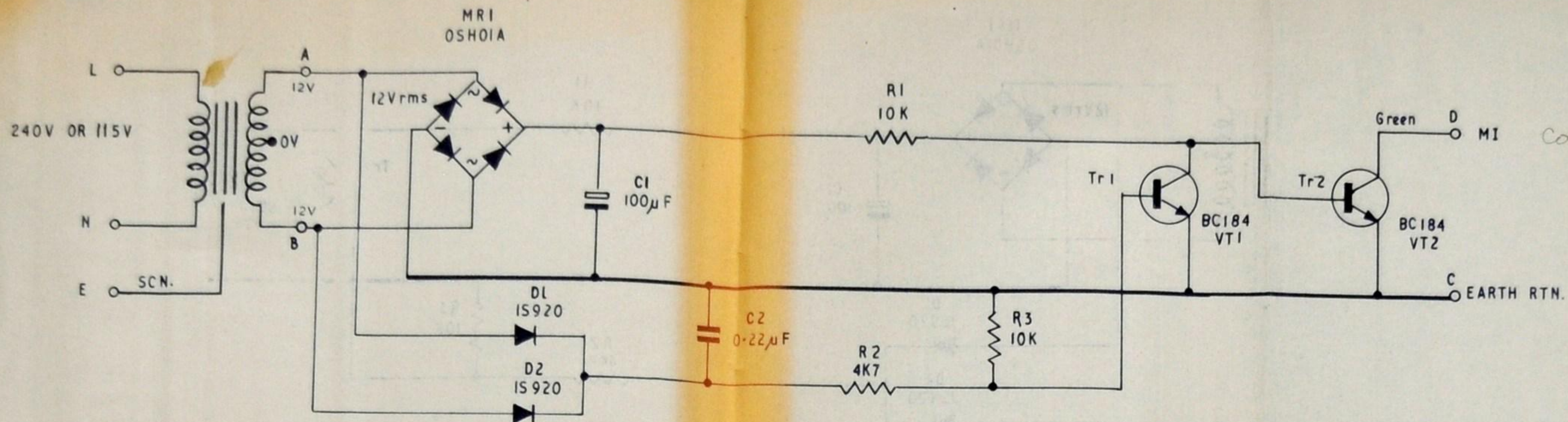
THE OTHER DDM BACK-UP CARD
CIRCUIT DIAGRAM

PCB 268

REF 1239

ISSUE A

6A01244



NOTE

FOR 115VOLT SYSTEM A AND B TO BE WIRED ACROSS SECONDARY (12V TO 12V). FOR 240VOLT SYSTEM TAKE A TO 12V AND B TO 0V OF SECONDARY.

ALL RESISTORS $\frac{1}{3}W \pm 5\%$ UNLESS OTHERWISE STATED

RANK STRAND ELECTRIC

29 King Street London WC2

A DIVISION OF

RANK AUDIO VISUAL LIMITED

DIMENSIONS IN INCHES/MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES

IMPERIAL	METRIC
FRACTION $\pm \frac{1}{64}$ "	1 DEC PLACE $\pm 0.4mm$
DECIMAL $\pm .005$ "	2 DEC PLACE $\pm 0.1mm$

ANGULAR $\pm 0.25^\circ$

UNLESS OTHERWISE STATED

USED ON:-

DDM 2

SCALE

DRAWN

CHECKED

APPROVED

MATERIAL:-

FINISH:-

DATE

1.6.73

4.6.73

4.6.73

TITLE:-

**A.C. MAINS FAIL DETECTION CIRCUIT
DIAGRAM.**

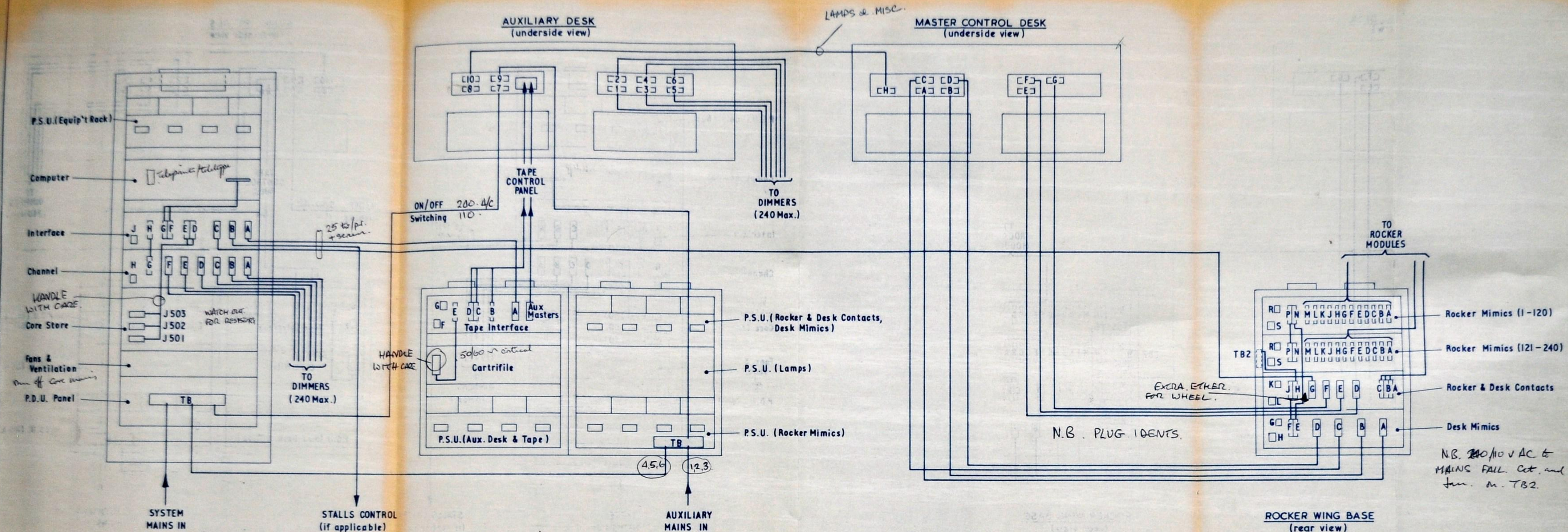
REF1242

PCB 284/1

ISSUE B

DWG. N° 6C1245I

REV. 1. C.N°



TITLE		
DDM.2 INTERNAL & EXTERNAL CONNECTING CABLES.		
B	3-5-73	Signature
ISSUE	DATE	SIGNATURE
IB 01646		

