

R T/T

Section 2

ELECTRICAL

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Sect. 2 Chap. 1

INTRODUCTION

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General

1. The DUET desk system is specifically designed so that hardware and functional boundaries are the same, i.e. a printed circuit card has a specific overall function within the system and is self-contained. With the exception of the program card any plug-in card can be removed without affecting the operation of other parts of the system. It is therefore advantageous to describe each printed circuit card or peripheral unit separately.

2. The heart of the system is the microprocessor with its supporting logic, all of which is contained on the processor motherboard (Section 2 Chap. 2). A bus system on the motherboard connects to all the plug-in printed circuit cards and these, where applicable, separately connect with interface sockets at the rear of the desk. Front panel controls connect to the motherboard to interface with the microprocessor.

3. All system options, whether plug-in printed circuit cards or separate units are described in this section. The OPTIONS section should be consulted to ascertain whether a particular option is applicable or not.

Levels of logic used

4. Levels of logic in the DUET desk fall into three categories and the specific circuit diagram should be consulted to determine which is applicable. Circuit diagrams show the operative edge of control waveforms where appropriate. The three categories are :

- (a) TTL logic where levels of $>+2.4V$ and $<0.4V$ apply
- (b) CMOS logic where levels of $+5V$ and $0V$ (nominal) are used and
- (c) certain analogue multiplex/demultiplex circuits which use $+15V$ and $0V$.

5. Additionally analogue levels produced vary between $0V$ and $+5V$ limits which, respectively, represent zero and full and dimmer lines are from $0V$ to $-10V$

CMOS Technology

6. The DUET system makes considerable use of complementary metal oxid semi-conductor (CMOS) technology. Briefly this means that logic gates

are constructed using the complementary operation of cascaded pairs of npn and pnp field effect transistors.

7. The main, but not the only advantage of this is the low power consumption. Any gate of this type consumes no power when in a settled state, only at the time of switching is current drawn and power consumed. Power consumption increases as operational speed increases but with modest operational speed heat conditions are minimised and design density can be increased. N.B. CMOS devices are extremely static sensitive and should only be handled in the prescribed manner. For details consult the static sensitive warning in the preliminary pages.

Hexadecimal numbering

8. A hexadecimal system of numbering (i.e. counting up to 16) has been adopted for DUET. Whilst this is mainly concerned with specifying addresses and is therefore primarily a programming tool, it does occur on certain of the circuit diagrams pertaining to the following chapters.

9. There are 16 address lines which can be considered as four groups of four lines. Four binary lines can be expressed in decimal as a count from 0-15, but in hexadecimal 10 to 15 are abbreviated to one character.

Hexadecimal counting follows a simple alpha-numeric sequence progressing from 0-9 and continuing from A-F. 16 binary address lines are thus expressed as four hexadecimal digits. (Table 1)

Address areas	Multiples of 1K						Addresses within each 1K									
Address bit no.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
Decimal	0						7						15			
Hexadecimal	0						7						F			

Table 1. Hexadecimal conversion example

10. In comparing hexadecimal numbering with 1K areas of address decoding (those areas of 1024 addressable bytes of data most commonly handled by memory devices) it is the second hexadecimal digit which counts 1/4 K areas. Multiples of four; 0, 4, 8, C in this second position therefore designate a 1K block. For example the 0K address area extends from 0000 to 03FF and the 1K address area from 0400 to 07FF. The example shown in Table 1 is thus the highest address in the 1K area.

Motherboard bus

11. Intercommunication between the microprocessor and program, memory and interface cards is conducted along the motherboard bus system. This has twelve identically wired card slots which allow considerable interchangeability of cards within the twelve slots.
12. Positions 7, 8 and 9 are allocated for memory card use starting with 4K^{capacity} in position 7 and building up to 24K ^{capacity in positions 7-9 (chap 4, table 1)}. Positions 10, 11 and 12 are allocated for channel cards on a progressive basis, starting at position 10. Unused slots at this end of the bus, together with slots 1-6 can be used by any ^{other} card as required.
13. Full details of pin to pin wiring, the signals carried and a description of their use is given on the block schematic diagram at the beginning of the CIRCUITS section.

Sect. 2 Chap.2

PROCESSOR MOTHERBOARD (1600)

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General

1. The principal element on the motherboard is the microprocessor which runs the system control program. This program is contained in permanent memory on a plug-in program card. Battery maintained read/write memory cards can also be added to provide lighting memory, as can channel output cards to interface to external dimmers.

2. Associated with the microprocessor on the motherboard are switch, lamp and display interfaces to allow the operator communication with the control program, and an analogue fade processing network to calculate and output the playback fades. Description of these areas also includes their associated panel controls and wiring.

3. Motherboard description is written with reference to the motherboard functional block diagram (fig.2.2.4) and to the three sheets of motherboard circuit diagram. Text support illustrations are included where considered necessary.

MICROPROCESSING

Circuit diaq.sh.1

Concepts

4. The microprocessor (MPU., IC69) supports the control program, with read-only memories (ROM) holding program instructions and random access memories (RAM) used for temporary storage and retrieval of data. A peripheral interface adaptor unit (PIA) is used to bridge between the microprocessor and the processing logic.

5. The MPU and PIA are complex items which are described in outline in the relevant descriptive areas with particular emphasis on their use within DUET. Product information on the microprocessor system used (Motorola 6800) is contained in the APPENDIX section.

6. The MPU can be looked upon as the master controller, executing the program by performing a series of tasks involving both logical decisions and calculations. To this end it produces (and varies through the program) addressing sequences.

7. The PIA is subsidiary to the MPU and is used by sub routines associated with the fade processing.

8. The memory devices are fairly straight forward in operation :

- (a) A ROM contains fixed data at each of its addresses, which can only be read out on a non-destructive basis
- (b) A RAM can have data written into it and read from it, but this data is only held as long as power is maintained.

Microprocessor interface

9. The MPU generates an address bus of 16 bits, it inputs and outputs a data bus of 8 bits and also responds to and generates a variety of control lines. Microprocessor interfacing is at standard TTL levels.

10. Microprocessor control inputs and outputs, as used by DUET, fall into two categories; those used in the control of the processor itself and those generated by the processor on the control bus. In the first category are the clocking timing and resetting signals provided by the system and applied to the microprocessor. In the second category are those signals with which the MPU controls, and is controlled by, the various parts of the overall system. These two categories are not completely self-contained and the next two paragraphs (which list these signals) include duplications.

Microprocessor control signals

11. (a) The clock for the system operates at a minimum period of 1.1 μ S. It consists of two phase, non overlapping pulses - $\phi 1$ and $\phi 2$.
- (b) Reset initialises the microprocessor (as well as the interfaces) and forces a restart of the program at the user defined starting address.
- (c) Data Bus Enable (DBE) removes the data bus from its high impedance mode. It is the complement of the ϕ clock.

Microprocessor bus control

12. (a) Clock for the microprocessor bus is a buffered version of the system - generated $\phi 2$ clock.
- (b) Reset is required by the system to insure an organised restart.
- (c) Halt, synchronised by the clock generator, can be used to stop the microprocessor, and place the data, address and relevant control lines into a high impedance state, allowing an external device to gain control of the bus.
- (d) Interrupt request (IRQ) is generated when an external device event occurs, requiring the normal program to be interrupted and a special service routine to be performed instead. The MPU will normally allow the interrupt at the end of its current instruction, but this is controlled by bit 4 of the condition code register (para 13(e)).
- (e) Non-maskable interrupt (NMI) is similar to IRQ except that the MPU must allow the interrupt at the end of its current cycle (para 13(e)).
- (f) Read/write (R/W) defines the direction of data transfer.
- (g) Valid memory address (VMA) indicates that a data transfer will take place on the current cycle.
- (h) Bus available (BA) acknowledges that the data address and control lines are in their high impedance mode.

Microprocessor registers

13. The MPU contains three 16-bit registers and three 8-bit registers all of which are used in the execution of the DUET program. These are :

- (a) Program counter, 16-bits, which points to the next program instruction address.
- (b) Stack pointer, 16-bits, which contain the address of the next available memory location in the stack. This stack, located in RAM, is used to contain the return address for sub routines and also the original processor state whilst servicing interrupts.
- (c) Index register, 16-bits, which is used to store the memory address for indexed mode addressing.
- (d) Accumulators A and B, 8-bits each, are used to hold operands and results of an arithmetic calculations.
- (e) Condition code registers, 8-bits ($\phi 0-7$) with bits 6 and 7 at logic 1. This indicates the results of an arithmetic calculation as follows :-
 Bit 0 - Carry (from bit 7 of the accumulators)
 Bit 1 - Overflow
 Bit 2 - Zero
 Bit 3 - Negative
 Bit 5 - Half carry (from bit 3)
 Additionally, bit 4 is the interrupt mask bit, 0 = IRQ and 1 = NMI (para 12(d) and (e)).

Clock and reset

14. Clocking is based upon a crystal oscillator operating at 10 MHz. This is followed by a divide-by 16 counter (IC78) operating together with divide-by-two D-type bistables (IC73,74) and discrete components to produce two anti-phased, non-overlapping 0V/5V clocks, designated 01 and 02. 01 is solely for microprocessor use while 02 is used both by the microprocessor and the rest of the system. Data bus enable (DBE), used by the microprocessor, is at TTL and is produced by IC74 from the 02 clock timing.

15. The reset pulse is the product of a compound voltage sensing circuit (VT58 to VT64) monitoring all the motherboard (and system) dc supplies (+15V, -15V, +5V). Failure of any supply thus causes a reset action. This is the case at the time of switch-on. Manual reset can also be effected by pressing the PRESET push on the motherboard. An LED within this switch indicates, however the reset is incurred.

Bus control

16. Microprocessor generated address lines A0-A15 together with control signals read/write (R/W) and valid memory address are under the control of the microprocessor - produced signal, bus available (BA) (IC 65, 75, 80). During microprocessor operation BA keeps the bus lines open. Only when the microprocessor receives the HALT signal (IC73) does BA become active and release the address and data bus, R/W and VMA.

17. The data bus on the motherboard is gated at two junctions to organise correct directional flow of data in accordance with the read/write cycle operation. These two junctions are where the data bus is accessed by the MPU (IC63,64) and where the data bus is accessed by the motherboard peripheral devices (IC56,57). In this latter case address bits A12 to A15 inhibit motherboard data bus access at address locations above those allocated 0K-3K (para 20).

Address buffering

18. Address buffering separates the address bits 0-9 (specific addressing within each 1K block of addresses) used by the motherboard peripheral devices from the address bus (IC37,43). The address bus itself is buffered from the MPU by the BA controlled gate, (IC65,75,80) (para 16).

Address decoding

19. Address decoding for the motherboard uses a section of a 4-line to 10-line decoder (IC50) arranged as a 2-line to 4-line decoder. Address bits A10 and A11 are decoded from the binary representation of the 0K to 3K address area into four 1K address area control lines. Address bits A12 to A15 inhibit motherboard operation at higher addresses.

20. Within the motherboard the following address block allocations apply :

- 3K - Contacts, mimics and display interfacing
- 2K - Fade processing interface
- 1K - } Random access memory for general MPU use
- 0K - }

Random access memory (basic program)

- (21. The motherboard contains 2K (blocks 0K and 1K) of 8-bit random access memory (IC36,41,42,48) which is used by the microprocessor in carrying out the basic program. Data areas contain
- (a) Channel stores (A,B,T and S etc.)
 - (b) Stack data
 - (c) Temporary data areas (flags,partical products,etc)

CONTROLS AND MIMICS

Circuit diag.. Sh.2

Control and mimic address decode

22. Control and mimic address decoding consists of a straightforward 4-line to 16-line decoder (IC38) gated by CLK and the 3K address area line. It decodes the binary address lines A0, A1, A2 together with R/W so that, of the 16 outputs, the seven associated with the mimic displays (M1-M7) operate during write-time and the eight associated with contacts (CON 0 to CON 7) operate during read-time. The zero line output is used as a test point.

Contact selection (push switches)

23. Selection of required operations is carried out from the front panel. In the interest of descriptive continuity, control selection is considered here (as well as in the front panel description, chap. 2.9).

24. The front panel motherboard contains a seven by eight diode matrix. CON 0 to CON 6 is applied to this matrix in the seven bit plane and output, CON D 0 to CON D 7, is taken from the eight-bit plane. Bridging the matrix intersections are the push switches, each with a series diode to prevent reverse current flow. CON 0-7 (via buffering, VT5 - VT12, and a data gate, IC17,18) are put onto the data bus D0 - D7. Thus there are seven bytes, each of eight bits which carry the push switch selection information. An eighth byte, contiguous with these seven and gated by CON 7 is used by eight bits representing wheel movement (para 31).

Wheel operation

- (25. An encoder, contained within the front panel wheel assembly produces, when the wheel is rotated, two square wave outputs 90° apart. From the timing relationship of these two signals can be determined whether the wheel is moving up (away from the operator) or down (towards the operator). The repetition speed of the pulses represents the speed of wheel movement, and a count of the pulses determines the amount of movement. There are 256 cycles per complete revolution of the wheel providing four edges per cycle which enables 256 pulses to be derived from a 90° quadrant of wheel movement. Based on these parameters, logic on the motherboard encodes wheel movement into an 8-bit 2's complement value.

Wheel movement calculation

26. Wheel calculation logic is independently clocked at a frequency of 50KHz, a period of 20 μ S. The incoming $\emptyset 1$ and $\emptyset 2$ signals are square waves phased 90° apart. By checking the continuing relationship of $\emptyset 1$ to $\emptyset 2$ and comparing the directional change of a waveform edge of one \emptyset against the steady state of the other it is possible to build up a truth table defining forward and reverse wheel movement.

\emptyset CHANGE	\emptyset STEADY STATE			
	$\emptyset 1 = 1$	$\emptyset 1 = \emptyset$	$\emptyset 2 = 1$	$\emptyset 2 = \emptyset$
$\emptyset 1$ UP			REV	FWD
$\emptyset 1$ DOWN	NOT VALID		FWD	REV
$\emptyset 2$ UP	FWD	REV		
$\emptyset 2$ DOWN	REV	FWD	NOT VALID	

Table 1 Wheel movement truth table

27. The 16 sections of table 1 are converted in binary form by using four clocked latches (IC66). Two latches give a first-sample of the two inputs and then feed back to the other two which give a second sample when next clocked. Four outputs giving 16 comparative possibilities are thus produced and are used to address two multiplexers (IC60,67).

28. These multiplexers are used essentially as decode switches, applying the OV input to either an UP rail or a DN rail. The eight invalid comparasions of table 1 (when like is compared with like) are not connected on the multiplexers.

29. Next comes two serially - connected up/down counters (IC44,51), wired to count each time they are enabled by the UP or the DN rail. Count direction can be reversed by DN, UP being the natural mode. The count output is in 8-bit binary form. When counting down the starting state of all 0's changes to all 1's and subsequently bit 7 is used as the direction bit (1 = down).

30. Whichever direction of count is defined it must not exceed the counting capability of the counter. Exclusive - OR gating (IC45), linked in with the counter enable line (IC52), ensures this and prevents counting beyond 120 pulses in either direction.

31. Data is gated out through transistors VT19-26 by CON 7 to share the access path to data bus with the contact selections (para 24). The trailing edge of CON 7, via C5 and R140, is used to reset the up/down counters so that each access reads the count of the wheel movement since the previous access.

Buffering and data gate

32. The eight bytes containing front panel switch selection and wheel movement data are buffered by transistors VT5 to VT12 and gated onto the data bus during read-time when the MPU is operating in the 3K address area.

Data latches for mimic and displays

33. Mimics and displays on the front panel are driven during write time in the 3K address area. Address decode lines M1 - M7 are applied to seven multiple latch elements (IC 23, 26, 31, 35, 40, 47, 54, 61) on their clock inputs. Each element contains four or six latches with common clock so that 6 or 8 data bits are latched at the seven addresses. It should be noted that coding of mimic drive is arbitrary (to aid the program) and in most cases differs from the contact coding of the same function (see address map in PROGRAM section).

Display drivers

34. Mimic outputs (those front panel pushes which have internal illumination) are transistor driven following data latching. Numeric displays are driven by 4-line BCD to 7-segment decoders (IC 39, 46, 53) to drive each segment of each numeral. The hundred figure of the channel/memory control number is transistor driven as are the two parts of the plus and minus characters.

Blink Drive

35. The blink function is a mimic bit which is continuously cycled by the program and gated with the appropriate warning mimic driver to cause the warning mimics to blink. Transistor drive (VI 31, 32) applies it to the warning (triangle) LED indicator on the front panel and the decimal points of the channel/memory numeric indicator. The blink program output also goes to the circuits providing channel decode and drive to the channel mimic LED display, and to the control bus for use by the VDU.

FADE PROCESSINGOutline requirement

36. The requirement of fade processing is to effect a smooth transfer of stage lighting from one lighting state to another. One lighting state may be zero, in which case a straightforward fade is executed, either up or down. Where two lighting states are defined, however, the process of bringing the new state up while taking the old state down must be achievable without causing a 'dip' in overall stage lighting. This is known as a dipless crossfade.
37. A particular structure accommodating the manual (A and B) and timed (T) faders into a program controlled system culminating in the output (grand master) fader control is used. Additionally, flash (full or out) and external manual fader wing provisions are incorporated. Fig. 2.2.1 shows a broad outline of the system structure used by DUET. It should be noted that as the hardware operates under program control, utilising the same elements several times within a routine, Fig. 2.2.1 is highly idealised. The calculation performed sequentially for each fader channel is shown in Fig. 2.2.2.

(Figs 2.2.1 & 2.2.2 to go in-text as near here as possible)

The peripheral interface adaptor

38. Fade processing revolves around the peripheral interface adaptor (PIA) and a sequence of 13 program addressed digital to analogue conversions. A channel sequence of operations has to be evolved and fitted into an overall fade processing cycle so that individual channel requirements can be implemented whilst also being subjected to levels set by the faders.

39. To accomplish these objectives the PIA uses its peripheral interface bus A to output the current channel number being processed (CHN0 - CHN6) and its peripheral interface bus B as individual input/output flags. Bits B1 to B5 of this highway are outputs which control fade processing and bit 7 is an input used in analogue to digital conversions. Both highways interface (via internal control and direction registers) with the data bus D0 to D7 and hence with the main program.

40. The PIA operates at four addresses in the upper half of the 2K address area. Address bit 1 defines whether the data bus is routed towards peripheral bus A (A1 = 0) or peripheral bus B (A1 = 1) and address bit 0, in conjunction with bit 2 of the control register, which is programmed (para 42,46), determines internal direction and routing. Data handling registers within the PIA make its operation, as viewed from the microprocessor that of four memory locations which are treated in the same manner as any other read/write memory. These registers are :-

- (a) Peripheral register A (PRA)/Data direction register A (DDRA)
- (b) Control register A (CRA)
- (c) Peripheral register B (PRB)/Data direction register B (DDRB)
- (d) Control register B (CRB)

Peripheral register A

41. PRA is the channel number register, with all bits programmed as outputs. It contains the channel number of the channel currently being processed. During a fade processing routine it is initially loaded with the top channel, then successively decremented until it underflows, thus indicating that the last channel has been processed and transferred. (N.B. Channel 1 - all 0's)

Control Register A

42. The bits loaded into CRA as part of program routine have the following functions.

Bit	Set to	Function
0,1 (2)	0,0 (0)	Not used Data bus accesses DDRA to control the transfer direction of subsequent byte through the PRA
2 3,4,5	1 1,0,1	Data bus accesses PRA for transfer Produces CA2 at read-time to generate a strobe to accompany the PIA bus A. This strobe signals that all the fade processing has been completed for this channel, that the analogue levels have settled and that the channel number is about to be decremented

Data direction registers A and B

43. The DDR's are used to establish each individual peripheral bus as either input or output. This is accomplished by having the program write 0 or 1 into the eight positions of the DDR when switched by bit 2 of CRA/CRB. 0 or 1 causes the corresponding peripheral data line to function as input or output, respectively.

44. DDRA will thus always be loaded with eight 1's and DDRB with seven 1's and a 0 in the bit 7 position.

Peripheral register B

45. PRB is the flag register with bits 0-6 programmed as outputs and bit 7 programmed as an input. It is loaded with the flag store for each channel before it is processed. The use of these eight bit is fully covered during description of the fade processing routine and its implementation. They are only briefly mentioned here.

Bit 7 is the result of the comparison of the output D/A level and the current analogue signal. The comparison is digitised ; 0 if D/A > analogue, 1 if D/A < analogue. (para 48))

Bit 6 Program use

Bit 5 All channels with this bit set are under channel control and are set to blink on the LED mimic. (para 67,70)

Bit 4 Is set to denote a down-fade for the particular channel. (para 55)

Bit 3 These bits specify which fader analogue or stage

Bit 2 level is to be digitised by the program (para 66, table 3).

Bit 1 Set if the channel is ON (> 1% lighting required) and used by the LED mimic card to illuminate the LED for the particular channel.

Bit 0 CHANNEL test point. Keyboard selection channel number flag.

Control register B

46. The bits loaded into CRB as part of program routine have the following functions :

Bit	Set to	Function
0,1	1,0	CB1, resulting from the system 4mS timer multivibrator (but inhibited by CB2, see bits 3,4,5), produces IRQB1, thus interrupting other system operations to update the MPU with a real time clock.
(2	0)	Data bus accesses DDRB to control the transfer direction of the subsequent byte through PRB
2	1	Data bus accesses PRB for transfer
3,4,5	0,1,1	CB2 is produced. This is used externally to the PIA to inhibit the 4mS timer multivibrator from producing CB1 and prevent the multivibrator from retriggering until CB2 is released so that any waiting interrupt is accepted. This inhibit is used so that PRB can be read as part of the A/D process without inadvertently clearing an interrupt request. See above. The next interrupt is the result of the 4mS multivibrator.
(6	-	Not used.
7	-	Used to indicate the production of IRQB1 (see above). CB1 sets bit 7 to 1 which in turn sets IRQB1. It is cleared by reading PRB.

Fade processing routine

47. Every fade processing cycle (which starts up to 36mS after the start of the previous cycle and takes as long as necessary) goes through a fixed routine to update the level of each channel in use. It is necessary to understand this routine before contemplating the fade processing logic, as the purpose of this logic is to support the routine. The following paragraphs and Table 2 explain this routine which is built around and implemented through a hardware structure of 13 analogue registers (para. 56).

(Table 2 to be inserted as near here as possible)

48. Firstly the fader FULL reference level is output then the current fader levels are digitised. This is done on a bit-by-bit basis for the A/B UP, A/B DN and the T faders through a selection circuit under the program control of bits 2 and 3 of PRB within the PIA (para 66). This successive approximation digitising process is the comparison (PRB 7) of the analogue level (fader setting) against each digital bit level, starting at bit 7 and proceeding in steps to bit 0. If the fader setting is above 50% of full then bit 7 will be set as a 1 for subsequent tests, if less it will be set as 0. Similarly bit 6 (representing 25%) will be tested with or without bit 7 as above and so onto bit 0 which represents 0.4% approx. Thus an accurate 8-bit digital representation of the three faders is built up in only 24 tests and retained in program storage.

49. Next these digital representations of fader levels, together with their complements, are re-output to six of the fade processing analogue registers as the current fade process and held for the duration of the cycle.

50. The PIA and fade processing logic now goes through as many channel cycles as there are channels, starting at the top channel and ending after channel 1 is processed. Each time the flag, A, B, T and S store contents for that channel are brought from their locations in RAM and output (in that order). A, B, T, S go to their fade processing registers causing the crossfade calculation to occur. (Fig 2.2.2) The output of this calculation is applied to the top of the GM fader which delivers a STAGE level applicable to that channel. This becomes the channel analogue level associated with that particular channel. It also is digitised if necessary, either as part of a regular 10 channels per system cycle to maintain a current stage store for use on the VDU mimic, or on a regular once per cycle basis for the particular channel being metered. Digitising is done by the same process as used by the fader levels (para 48).

51. When all channels have been thus processed the fade processing routine completes and the microprocessor attends to its other program requirements.

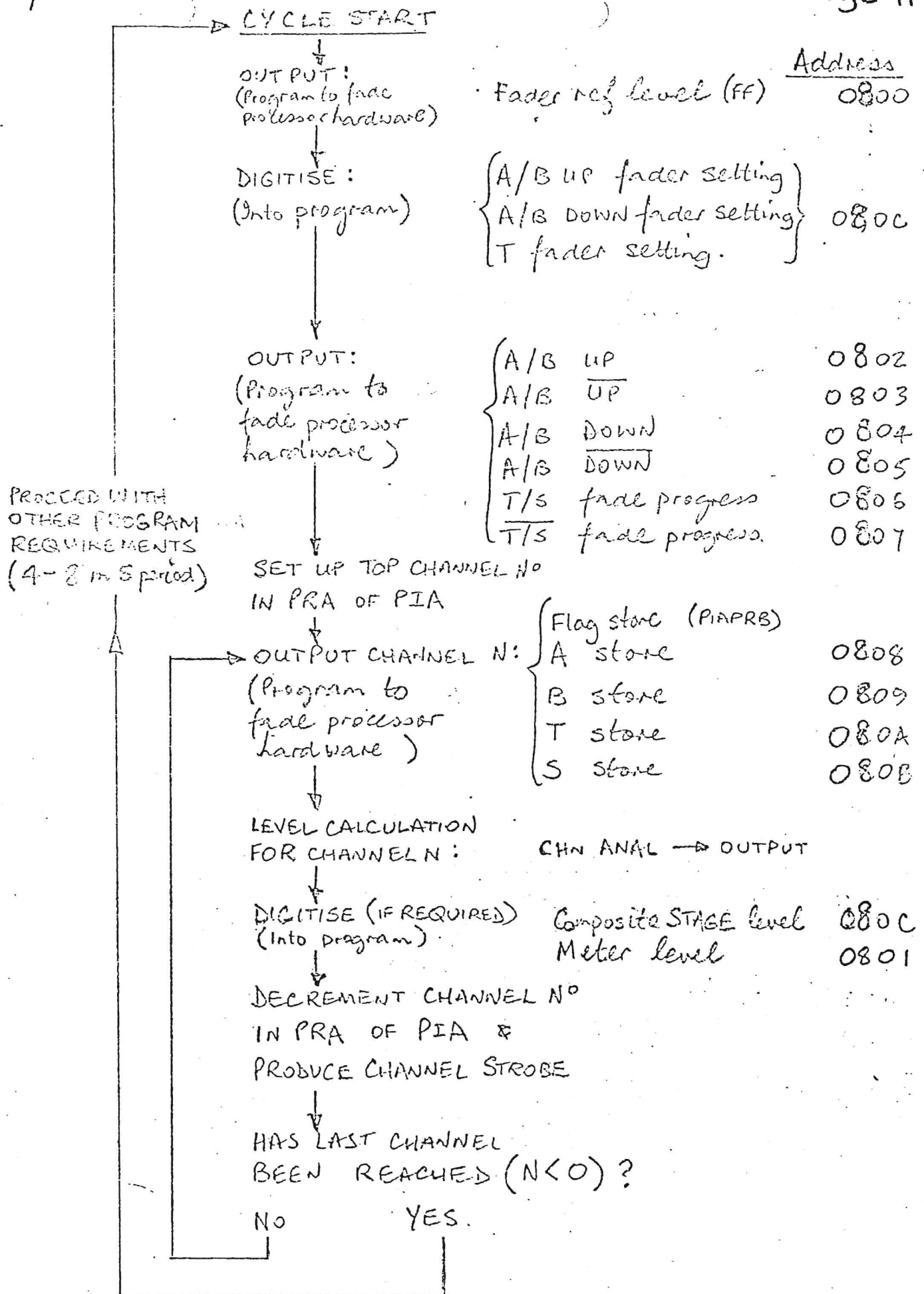


Table 2 Fade processing cycle routine.

Hardware descriptionClock control

registers are

52. The fade processing analogue registers are addressed in the lower half of the 2K address area. Processing timing is controlled by two monostables (IC12) of 1 μ S and 3 μ S duration such that :

(a) The SYNC pulse ensures that the CLK pulse is stretched to at least 1 μ S. This provides a delay of 1 μ S between the address latch change (which controls the analogue multiplexers) and the data latch change (which changes the analogue level).

(b) The 3 μ S monostable stretches the inhibit on the analogue register multiplexers. These are only output once per cycle so that the analogue level has settled before being sampled.

Address and data latches

53. Address and data information for fade processing is latched (IC 20, 21, 22) under the control of the SYNC 1 μ S monostable or the stretched CLK resulting therefrom (para 52).

Address decoding

54. Address decoding (IC 13, 14, 15) converts the addresses A0-A3, latched by IC 20, into appropriate control code for IC 7-10. The address decoding can be considered in three parts.

(a) Addresses 0-7 are used to set up the system parameters used by each channel.

(b) Addresses 8, 9, A, B are output each cycle with the store levels for A, B, T, S. When output in that order they allow the crossfade calculation to occur. Multiplexer IC 8 selects the appropriate mastering level, whilst IC 9 allows the earlier A or T result to be added to the next output. Demultiplexer IC 10 is enabled to save the result.

(c) Address C is used as the trial output for comparison with the selected analogue level for D/A conversion. Addresses D and are unused and address F is used to provide a test signal every system cycle for oscilloscope triggering.

55. In order to ensure that a channel on the down part of the main crossfaders is correctly controlled, the PIA is loaded with the flag S if the channel is on a DOWN fade, and causes multiplexer IC to switch to the correct fader mastering.

(fig 2.2.3 to go as near here as possible)


Digital to analogue  fade registers

Fig 2.2.3

(56. This is basically a configuration of 16 analogue registers, shown as one block on the functional block diagram fig. 2.2.4 and expanded in fig. 2.2.3. It is advantageous to consider it as one entity, as it is the central hardware structure concerned with supporting the fade processing routine.

57. Referring the fade processor cycle routine (Table 2) to the hardware (Fig. 2.2.3), the first consideration is the digitising of the fader levels. Multiplexer 1 (IC⁸) is addressed so that the FULL reference (5V) is chosen and used as a digital to analogue controller for IC¹⁶ which is input by all 1's from the program. The analogue output thus represents 'full' and through a summing circuit (VT1,2 IC⁴) is applied to demultiplexer 1 (IC⁹). IC⁹ is addressed so that the analogue output becomes the FADER TOP supply for the A/B UP, A/B DN and T faders. The fader levels are digitised using a successive approximation technique (para 48) and placed in program store.

58. Next the digitised settings of the A/B faders and the progress of the T/S crossfade (together with their complements) are successively output from the program. Then they are digital to analogue converted (IC¹⁶), individually selected by demultiplexer 1 and the analogue levels held on their individual storage capacitors for the remainder of the cycle (C14 - C19). The meter level for the currently selected channel is similarly treated.

59. Having set up the cycle parameters using 8 of the analogue registers the other eight (demultiplexer 2, IC¹⁰ and multiplexer 2, IC⁷) are now used repetitively per channel as described in para 54. Channel crossfade calculations (fig. 2.2.2) are performed at this stage.

for
60. Six steps occur ~~each~~ for each channel. Firstly the flag store is loaded into the PIA PRB, then it is output from the program and multiplied by either A/B UP or A/B DN. Multiplexer 1 (IC⁸) is addressed so that the appropriate multiplier is applied to the ref. input of the D/A converter (IC¹⁶) to perform this step. The result ($A \times A/B$) is temporarily stored on C²² by demultiplexer 2 (IC¹⁰).

61. Next the B store is output from the program and this is similarly multiplied by the appropriate complement fader level, A/B UP or A/B DN through IC⁸ and IC¹⁶. The result ($B \times A/B$) now has the previous result ($A \times A/B$), passed by multiplexer 2 (IC⁷), added to it by IC⁴. This gives a final A/B product of $(A \times A/B) + (B \times A/B)$ which is passed through demultiplexer 2 (IC¹⁰) and stored on C²¹.

62. Steps four and five perform the same calculation for the T/S fade calculation, its output being stored on C²⁰. The two results, representing fade progress from A to B and from T to S are combined on a highest-takes-precedence basis (IC⁴) and applied to the GM (output) fader as its top reference level.

63. Finally the resultant output from the GM fader is digitised and placed in program store in order to keep an up to date record of the STAGE level. Because this is a lengthy process in terms of channel time only 10 channels are selected for this process each cycle, together with the currently metered channel. Output level digitising uses the same process as the fade digitising (para 57); FULL is selected as the D/A reference and 1/2 LSB offset used in the successive approximation technique (para 48).

Fader controls and analogue to digital processing

64. Fader controls on the front panel have their drive (top) levels adjusted by the processes described in the previous paragraphs. Fader wiper levels are input to the motherboard and undergo the following processing.

65. The A/B UP, A/B DOWN and T fader levels are all applied directly to a multiplex selection stage (IC²⁶) while the output (GM) fader, after being combined on a highest-takes-precedence basis with the analogue output from the manual fader wing (if applicable) (IC²⁵) become the channel analogue signal. Channel analogue is the prime output along with the current channel number and is passed to the channel boards to be demultiplexed. It is also known as STAGE, and as such is also applied to IC²⁶.

66. The multiplex selection organised by IC²⁶ is addressed by bits 2 and 3 of peripheral bus B of the PIA (Para 45 and Table 3). The required fader level is thus selected for the digitising process at the A/D comparator (IC²³) using the successive approximation technique (para 48). The comparison is sensed at by bit 7 at PRB of the PIA.

PRB OF PIA		SELECTION FOR DIGITISATION
BIT 3	BIT 2	
0	0	STAGE level, whose parameters have just been output
0	1	A/B UP fader
1	0	A/B DOWN fader
1	1	T fader

Table 3 Digitisation selection addressing

Flash facility

67. When the flash switch is engaged, either FULL or OUT, the operation is encoded (by transistor VT²⁷ on the motherboard) into the front panel matrix format, and hence read as a contact by the program. It thereby allows the bringing under control of all those channels needing to be flashed. Bit 5 on the peripheral bus B of the PIA, representing the channels selected for channel control, gates the flash commands (IC¹¹). FULL is applied to the GM TOP line and OUT is applied to the GM FADER wiper line.

Program Cycle

68. A fade processing recurs up to every 36mS. This is controlled by a 4mS multivibrator IC 27 which provides a regular interrupt via CB1 and PIA action for fade timing and cycle timing control. Normally, at the completion of an output cycle, 1 to 2 periods (4-8mS) is allowed for other processing (e.g. contact / mimic, VDU updating etc.) before the next output cycle is commenced. PIA CB2 output is used to inhibit the multivibrator and interrupt triggering during an A/D conversion.

Channel Strobe.

69. Monostable IC 24, triggered by CA2 from the PIA, produces a 70uS pulse timed to start 2uS in advance of the channel bus lines being changed. This signals that the analogue levels have settled for the channel number now output, but both will shortly change and should be latched now. At the end of the 70uS the new channels number and level will be set and sampling may commence.

Mimic-on-control

70. LED mimic displays are driven by program control of bits 1 and 5 of peripheral bus B from the PIA which contains the flag store for each channel. These bits designate, for each channel, that the LED mimic display should be on and whether it should blink.

Act 2 Chap 3

PROGRAM CARD (1601)

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General

1. There is one program card used within the DUET desk system. It plugs into the motherboard bus structure and provides all the instruction data to enable the microprocessor on the motherboard to perform its normal control program. The program card is normally plugged into slot 1 but can be plugged into any of the twelve slots on the motherboard, bearing in mind that slots 7,8 and 9 are also memory card allocated and slots 10,11 and 12 are also channel card allocated (Chap. 4,7) but may not all be used for these purposes.

2. Description of the program card is made with reference to the functional block diagram, fig. 2.3.1, and to the circuit diagram.

Detailed description

3. Address block selection for the program card is achieved by exclusive -OR gates (IC14) comparing microprocessor addresses A13, A14, A15 with wired link selection AP13, AP14, AP15, thereby allowing card operation within the designated 8K address area, normally E000 - FFFF (Table 1). When the address matches and valid memory address (VMA) is true, clock (CLK) with read/write (R/W) enables two things to occur during read-time:

- (a) the 0K to 7K decoder (IC1) is enabled, thereby allowing the appropriate PROM to be addressed
- (b) the output control gate (IC15,16) is opened thereby allowing PROM data onto the data bus, D0-D7

Address Patch	AP15	AP14	AP13
E000 - FFFF	OPEN	OPEN	OPEN
C000 - DFFF	OPEN	OPEN	LINK

Table 1 Address area selection

4. A three-line to eight-line decoder (IC1) decodes the microprocessor address lines A10, A11, A12 to the appropriate one of eight integrated circuit PROM's (IC3 - IC10). One PROM is thus enabled to output the data programmed at the address defined by bits A0 - A9.

5. The PROM's used are electrically programmed and can be erased for re-programming by strong ultra-violet light. To avoid this happening do not expose the PROM's to strong radiation, sunlight or other source of ultraviolet. The PROM's are supplied pre-programmed. When on a card referenced 1601 S they contain the standard facility

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2.4.1

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Table

Memory card positions

1

General

1. Memory cards come in two capacity options, 4K and 8K, and normally accommodate 6 bits of memory on data lines D2-D7. They are allocated three slots within the motherboard bus structure, these being positions 7, 8, and 9. So a memory capacity ranging from 4K minimum to 24K maximum is possible. Wiring on the motherboard decides the order that the three cards positions are decoded within the microprocessor addressing area, and thus makes slots 7, 8 and 9 unique when memory boards are plugged in.

2. Memory cards must be inserted as in Table 1

Capacity	Posn 7	8	9
4K	4K	--	--
8K	8K	--	--
12K	8K	4K	--
16K	8K	8K	--
20K	8K	8K	4K
24K	8K	8K	8K

Table 1 Memory card positions

3. The motherboard wiring, in conjunction with exclusive gating with each memory card, ensures that the cards commence to be available at the following addresses

Card Slot

Starting address

7

16K (4000)

8

24K (6000)

9

32K (8000)

4. Description of the memory card is made with reference to the functional block diagram, fig. 2.4.1, and to the circuit diagram.

Detailed description

5. Address area selection is achieved by exclusive -OR gates IC5 comparing the microprocessor address with wired parameters from the motherboard and thereby only allowing card operation within the designated 8K address area. When the address is within this area, clock, together with valid memory address (VMA) enables three things to occur :

(a) the 0K to 7K decoder, (IC11) is enabled, thereby allowing the RAM to be addressed

(b) the input/output gate (IC3,4) brought under read/write (R/W) control thereby connecting the RAM with the data bus, D0-D7

(c) A 1uS monostable IC2 is triggered to slow the microprocessor. This allows for the slower response of the memory devices.

6. The RAM array is organised as eight 1K addressed columns by eight 1-bit addressed rows. For a 4K card only the first columns are filled ; for an 8K card all columns are filled. Columns are selected by the appropriate output of the 3 to 8 line decoder IC11 and address lines A0 to A9 are wired to all positions.

7. Each row is wired to one data line, D0 to D7, but since the usual memory requirement is only 6-bit, rows providing D0 and D1 are left unfilled. There are pull-up resistors on the memory device output lines and non-inverting data bus gates are used, causing the device data to be low-active. This ensures that missing devices return 0's when addressed.

8. Power for the RAM is backed up by three nickel cadmium rechargeable batteries which provide 3.6V. In the event of power failure or shutdown they ensure that memory contents are retained and data is not corrupted.

9. With +5V available it is applied through a series switch VT11 to provide the supply designated + BATT. Upon power failure VT9 and VT10 act to switch off VT11 and the supply is now provided by the battery via D8. At the same time VT9 switches off VT12 which provides, via VT14, a power fail drive which operates on the reset line. This inhibits the strobing of RAM addressing and the writing of data into RAM.

10. VT13 and associated circuit senses the level of the +5V supply. Should this fall below +4V (approx) VT13 switches and, via VT14, produces power fail drive.

11. Battery charging is achieved from the +15V supply via D4 and takes place whenever power is applied. Charging takes approximately 12 hours from a completely discharged state. Batteries are subsequently kept topped up by the normal process of having the equipment running and will last for a minimum of 1 month without power.

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General

1. There are two types of serial link card, F or R, which are within-desk options needed to interface the asynchronous data from the floppy disc unit or riggers unit options with the microprocessor program. Asynchronous data can be considered in this case to mean serial data of an intermittent nature organised by an independent synchronising standard. Both cards are functionally the same, the only difference being the program fitted and the baud rate selected.

Description is made with reference to the functional block diagram and the circuit diagrams.

2. The serial link card can be plugged into any of the twelve slots on the motherboard bus structure, bearing in mind two considerations :

(a) positions 7-9 and 10-12 are assigned to memory and channel cards, but vacant spaces at this end of the bus could be used.

Positions 1-6 are multipurpose, non-allocated slots.

(b) the ten-way flat cable from the desk rear connector must connect with the card.

3. The card contains an asynchronous control interface adaptor (ACIA) which transmits and receives serial data and control signals. 2K of program in two 1K PROMs provides a control program which is specific to the external device being interfaced.

Detailed description

Control functions

4. Address area selection for the serial link card is achieved by exclusive -OR gate (IC6,7) comparing microprocessor addresses A11-A15 with wired link selections AP11-AP15 thereby allowing card operation only within a designated address area. Address area selection enables three things to occur :

(a) the 2K or 1K decode of the card program is enabled and thus the program instructions can be read from PROMs IC14,15.

(b) the card data input/output gating is brought under read/write control

(c) the ACIA is partially addressed at CS3,1 so that it can subsequently be addressed at CS2. (para 5)

5. In order to economise on address decoding the ACIA is addressed in the last 3 bytes of the 2K PROM area and will respond to any of these addresses. This area is defined by address bits A3-A10 as applied to the AND-gate (part IC9) which produces CS2 and completes the ACIA addressing. At this time the card PROMs are inhibited.

6. Card program, preset into the two 1K PROMs, is output to the microprocessor for all but the last 8 bytes of the 2K address area. The microprocessor can read and write the required data and control when the ACIA is addressed at the final 8 bytes.

7. Data gating out of and into the card is on a read/write basis at clock (CLK) time during the selected address block (IC1,2,12).

8. Clocking, for the ACIA to handle the data to and from the external serial line device, internally generated. A crystal oscillator, followed by divider stages (IC18,19) produces nine baud rate frequency options which can be selected by links via a de-multiplexer IC20. Full details of baud rates available and the links needed to select them are on the circuit diagram.

ACIA operation

9. The ACIA operates when its address inputs CS0,1,2 are satisfied (para 4,5) and thereafter the microprocessor can converse with the ACIA on a read/write basis at two addresses defined by A0. The microprocessor sees the ACIA as two memory locations to be treated in the same manner as any other read/write memory. A0 and R/W define the following internal registers within the ACIA:

(a) control register	- write	- A0 = 0
(b) status register	- read	- A0 = 0
(c) transmit data register	- write	- A0 = 1
(d) receive data register	- read	- A0 = 1

10. The control register is an eight bit write only buffer which controls operation of the ACIA receiver, transmitter, interrupt enables and the request-to-send control line. The program sets up and controls this register as required.

11. The status register is an eight bit read only buffer which informs the microprocessor of:

- (a) the state of the input lines CTS and DCD
- (b) the status of the transmit and receive data registers and
- (c) the interrupt state of the ACIA.

12. When A0 = 1 a data byte for outputting can be transferred from the microprocessor to the transmit data register during write-time. It is subsequently converted from parallel to serial form for output.

Conversely, during read-time, a byte of data previously converted from serial to parallel form and held in the receive data register, is passed to the microprocessor. When a complete byte has been received from the peripheral unit it generates an interrupt request (IRQ) thereby asking the microprocessor to accept the data. By inserting link INTIP this can become a non-maskable interrupt (NMI) which establishes it as a higher priority, if required.

13. Output to and input from the serial data interface unit is via buffer stages IC21,22.

Riggers interface card

14. An additional interface card, located on the rear panel is used in conjunction with the (R) version of this card. This matches the 3V operating levels of the riggers control with signal and threshold levels of the ACIA (see

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General

1. A VDU interface card is required to feed mimic information from the microprocessor routine out to a video display unit, if the system includes this particular option. 2K^{of} microprocessor address^{space} is allocated to this particular operation in which instruction data can be read and character data can be written for display on a uniquely addressed position on the screen. The display consists of channel data, together with desk status information, all of which is converted by the card to a standard video output.

2. The VDU interface card is inserted into one of the slots within the motherboard bus structure. Any slot can be used, bearing in mind two considerations :

(a) positions 7-9 and 10-12 are assigned to memory and channel cards, but vacant spaces at this end of the bus could be used. Positions 1-6 are multipurpose, non-allocated slots.

(b) the video output cable from the desk interface socket must connect with the card.

3. Description of the VDU interface card is made with reference to the functional block diagram and to the circuit diagram.

Video display concepts

4. The video to be displayed is organised by the program and presented by the VDU interface card. The display unit is simply a CRT video monitor with its own power supply. The VDU interface card undertakes the following functions :

(a) At its allocated address area within the overall system the VDU

program is read by the microprocessor.

(b) The microprocessor computes the data required and deposits it as a character code in random access memory on the card.

(c) Internal timing, which defines line and frame scan timing, also co-ordinates data memory storage and retrieval and then controls its application to the character generator. Data display is now independent of microprocessor control.

(d) Characters are output as a series of dots in synchronism with line and frame time and are output to be built up by the CRT raster in the video display unit.

5. Display organisation should be considered on two counts; the composition of individual characters and the data presentation over the entire face of the CRT.

6. Individual characters are built up as a dot matrix five wide and seven high. An extra dot space is added for vertical character separation and three line spaces are added (one above and two below) for horizontal separation. Total character space is thus 6 dots wide and 10 lines high.

7. DUET video display unit presents 24 rows of data, each row containing up to 64 characters. Thus the usable CRT frame consists of 240 lines, each line having 384 dots.

Video presentation (when 50 Hz is the input supply) is traditionally 625 lines of interfaced information, i.e. odd lines are presented on one frame and the even lines presented on the next frame thus giving two interfaced frames of 312 1/2 lines. When 60 Hz is used 525 lines of interfaced presentation is the norm.

9. DUET does not use interlacing; it refreshes the entire presentation every frame. The frame thus consists of 312 lines from 50 Hz, or 262 lines from 60 Hz. As 240 lines are required for data presentation (para 7) there is (respectively) a surplus of 72 or 22 lines. A common line time of 64 μ s is used in both cases, of which 51 μ s is used to display the 64 characters, the remaining time being taken by 20 dummy characters.

10. So far overall times and useful times have been specified without consideration of the lost time incurred by line and frame flyback. These are absorbed into the surplus time and blanked, along with unused time. Total times are examined in Table 1

Line Timing		Frame Timing (50 Hz)		Frame Timing (60 Hz)	
Character space	Allocation	Character row	Allocation	Character row	Allocation
0-63	Data	0-23	Data	0-23	Data
64-69	Spare - blanked	24-26	Spare - blanked	24.0, 24.1	Frame sync pulse - blanked
70-75	Line sync pulse - blanked	26.0, 26.1	Frame sync pulse - blanked	24.2-26.2	Flyback time - blanked
76-83	Flyback time - blanked	26.2-27.1	Omitted		
		27.2-29.1	Flyback time - blanked		
		29.2-31.2	Spare - blanked		

Table 1. Line and frame timing

11. The counters which define the parameters of line and frame must also assemble the data for display only at the valid times. It must also, at the setting of a 50 Hz/60 Hz switch, be able to adapt the two frame requirements to a common data handling format. The following paragraphs describe how this is achieved.

Detailed description

Microprocessor interface

12. Links AP11-API5 (as selected during commissioning) define the address block within which the VDU interface card operates (IC3,5). Within this area read and write control (IC23), at clock time, allows the card program data in PROM to be read by the microprocessor and the required data from the microprocessor to be written into the card RAM.

Two-page organisation

13. The 2K of RAM is organised as two 1K pages each with its own data input/output gating and address line switching. The addressing is organised so that alternate characters along a TV line are contained in the alternate pages. This means that as character data is output along a line, it is taken from alternate pages each character, leaving the other page free for about 700 ns. During this time the other page is available for writing by the microprocessor, and it follows that any location in either page will not cause the microprocessor to wait more than two character spaces before a complete character time is available for writing.

14. The locally generated bit CTR0 is the controlling, switching and synchronising signal used during the two page operation. Ten two-way address line switches (IC27 to IC31) controlled by CTR0 alternately switch the two pages of RAM between A1-A10 and CTR1-CTR10. Data input and output of the RAM pages are switched between pages by CTR0 as is the write enabling (WE0, WE1) of the RAM pages.

15. Writing of a RAM page (IC11,12 and 16) commences with the input of a write request from the microprocessor on the R/W line in the defined address area. Two monostables (IC16) are triggered; the first produces a sync pulse of up to 3.5 μ s which it returns to the microprocessor, and the second produces a 200 ns write delay pulse which inhibits the start of a write cycle until data is settled. Clocking is the result of exclusive -OR gating A0 and CTR0 by part of IC4. This synchronises the beginning of RAM page availability by clocking bistable IC12.

16. This bistable, now clocked and set, gates the write-time signal from the character timing counters (para 18) and uses A0 to enable one of the two-page write enable signals (WE0, WE1) (IC11). WE0 or WE1 thus latch the microprocessor data into the RAM, synchronised by the timing of CTR0. When the write-time signal terminates the production of WE0 and WE1 it clocks the other bistable within IC12 (previously primed as the first bistable sets) and its output terminates the sync pulse thus allowing the microprocessor to proceed IC12 to clear.

Internal timing

17. The purpose of internal timing on the VDU interface card is threefold:

- (a) it provides a character addressing sequence to extract character data sequentially from the 2 page RAM
- (b) it provides line and frame synchronisation for the CRT in the display unit
- (c) it adjusts the timing used for CRT drive and applies to it to data handling (after it is read from the two-page RAM) in order to fit data presentation into the valid times (Table 1)

18. A basic frequency of 7,875 MHz is provided (by a crystal oscillator) as the basic dot rate frequency for character generation. The basic frequency is applied to a $\div 6$ counter (part IC24) which defines the number of dots within a character width. A bistable (half of IC26) is toggled at this divide-by-six frequency to provide a write-time pulse midway in a character space.

19. Having defined the number of dots per character the next two dividers (IC32, 33) provide a divide-by-84 count to define the number of characters per row. 64 counts of the 84 are generated as CTR0 - CTR5; these define the vertical space into which data is to be inserted. They are used by the RAM to provide the column address for the character read out. Decoding of CTR0 - CTR5 and an overflow bit defines the timing of other events within a line cycle, i.e. flyback, blank time etc. (Table 1).

20. A bistable (part IC26) sets at a count of 20 over the 64-count and clears down the line counters to start a new line. Another bistable (part IC43) sets at a count of 6 over the 64-count to provide drive for the lines-per-character counter (IC40) while simultaneously delivering a line sync pulse onto a composite line/frame sync line.

21. The lines-per-character counter (IC40) is wired to deliver a 16-count to the character generator and then trigger the character row-per-frame counter CTR6-10 (IC41 and part IC26) which is used by the RAM to provide the row address for the character read.

22. To differentiate between 50 Hz and 60 Hz operation,

a count jump is organised between the second line of count 26 and 27 (50 Hz) or 24 and 30 (60 Hz). In this way the line format is switched for 50/60 Hz operation while maintaining the displayed data in a suitable position.

23. And-gate IC35/6 decodes either row count 24 or 26, as enabled by controlled inversion of the 2's count by IC45/3. Frame blanking is provided at counts over 24 by AND-gate IC35/8.

24. The two bistables within IC44 are clocked two line sync pulses later (which uses up the two extra lines within the frame). The two counters (IC40 and 41) are reset to their starting points by one bistable while the frame sync pulse is produced by the other. IC43/5 controls the timing and length of the frame reset pulses clearing them at the end of a line sync pulse (para 20). The frame sync pulse is cleared two line sync pulse intervals later.

25. Frame sync pulse is combined with the line sync pulses to produce a composite sync line where line sync pulses are short (4.2uS) and frame sync pulses longer (5uS, approx). Composite sync is produced at IC43/9 by line sync decode (para 20). When frame sync is produced, the setting of IC43/2 is extended, via its preset input, which is driven by frame sync plus a row character decode of 12 at IC35/12. Frame sync, produced for two line sync pulse intervals, stops

between character counts 64 and 70. This is so that line sync circuits in the VDU can be refreshed even though a frame sync is current. The interruption is brought about by network C27 and R44 and the exclusive -OR action of IC34/8.

26. line blanking, defined by any count over 64 character widths, and frame blanking, defined by any count in excess of 24 character rows, are combined by IC34/11 to ^{become} a composite blanking instruction.

Character generation and output

27. The RAM information is refreshed as required by the microprocessor but is repetitively read out from the RAM every frame of CRT scan. CTR0 defines which page of the RAM is gated out and whether the microprocessor or screen display counters address the page. Outputs from both pages are gated together and referred to as VDO0-VDO7. (video data outputs).

Address	Character	Address	Character	Address	Character	Address	Character
0	@	10	P	20	Space	30	φ
1	A	11	Q	21	!	31	1
2	B	12	R	22	"	32	2
3	C	13	S	23	#	33	3
4	D	14	T	24	\$	34	4
5	E	15	U	25	%	35	5
6	F	16	V	26	&	36	6
7	G	17	W	27	'	37	7
8	H	18	X	28	(38	8
9	I	19	Y	29)	39	9
A	J	1A	Z	2A	*	3A	:
B	K	1B	[2B	+	3B	;
C	L	1C	\	2C	,	3C	<
D	M	1D]	2D	-	3D	=
E	N	1E	^	2E	.	3E	>
F	O	1F	1 (RH. 1 of 100's)	2F	/	3F	?

Table 2. Character generation PROM contents

28. Bits VDO₀-VDO₅ select one of 64 programmed characters. These consist of 26 letters, 11 figures 26 symbols and a space. Full details of character generator coding is given in Table 2. VDO bits 6 and 7 define special conditions which are program defined and are to be applied to the character defined by bits 0-5. These special conditions are :

	Bit 6	Bit 7
(a) normal video	0	0
(b) dim video	1	0
(c) blink normal video	0	1
(d) reverse video (black on white)	1	1

29. Latches (IC36,38) are used to keep control and data signals synchronous. VDO bits 0-5 then address the character generator (IC39) along with the ten-count output from the line-per-character counter (IC42)(para 21). The character generator contains the information to build the character, now that it knows which character is required and which line it is working on. It outputs, in parallel form, the six dots for that character line.

30. Two shift registers (IC46,47), serially connected, convert the character data from parallel to serial form at the final output. These registers parallel load the character generator PROM data for one bit time, then shift right the remaining bits for the next five dots while the character generator prepares the next character.

31. Of the special conditions specified in para 28, blink, together with blanking, inhibits the character generator, reverse is exclusive-OR gated to invert the serial pulses and dim applies an attenuation to the video at the output stage. In order to keep the dim and reverse signals synchronous with the video processing they are double clocked through sections of IC46 and IC36 respectively.

32. Video output is 1V at 75 Ω as delivered by VT1. VT2 clamps the output to 0V at sync pulse periods : at other times black level bias (0.3V) is produced by R47,48, D2; peak white bias (1V) by R49,D1 and dim attenuation (0.6V peak) by R50,D3.

(FIG 2.6.1 GOES HERE)

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DUET desk : 48-way channel card : functional block diagram	2.7.1

General

1. Channel cards provide 48 channel outputs from the motherboard channel bus input. This is achieved by sampling then holding the multiplexed analogue output for each channel on a capacitor, this is then used, via a buffer amplifier, to drive the dimmer. The cards are allocated three slots within the bus structure, these being positions 10, 11 and 12. The number of boards used obviously depends on the channel capacity of the particular desk; 36 and 48 channels only need one board, 60, 84 and 96 channels need two boards whilst 120 channels require three boards.

2. Motherboard wiring in connection with channel group selection logic on each channel card ensures that the following channel allocations apply.

<u>Card slot</u>	<u>Channel allocations</u>
10	1 - 48
11	49 - 96
12	97 - 120

3. Description of the 48-way channel card is made with reference to the functional block diagram, fig. 2.7.1 and to the circuit diagram.

Detailed description

4. Channel group selection within the card is accomplished by IC2, a four-bit binary adder. The motherboard wiring provides a fixed count for each board. When this is added to channel number (CHN₀ - CHN₆) applied to each board from the bus, it off sets the count of bits CHN₀ - CHN₆ and causes the adder to start at zero for channel codes of 0, 48 and 96. The binary decoder (para 5) is enabled at this time.

5. The current channel number and analogue level are sampled on C1 to C8 until channel strobe (CHN STB) occurs. This signals that the channel number and analogue is now correct but will change in 2µs. CHN STB (70µs duration) freezes the current data and drives decoder IC6 which, if correctly addressed for these channels, enables one of the six demultiplexing switches IC7 - IC12. These, in turn, enable one of the output capacitors C16 - C63 to be charged to the analogue level output by IC5. This can be between 0V (out) and -10V (full).

6. At the end of the 700uS CHN STB pulse the demultiplex switch is opened causing the current level to be held on its analogue sample capacitor and to drive the dimmer at this level until revised a microprocessor cycle later. The strobed gates IC1, IC3 are now re-opened to sample the data for the next channel to be output.
7. Channels are output in a downward progression starting with the top channel and decrementing through to channel 1 (CHN = 0). The sequence then pauses for 4 - 8 ms^{before} starting again.
8. Analogue demultiplexing circuits operate from a negative supply of -11V provided by zener diode D1. A comparison with this -11V and a fraction of the -15V supply (-12.2V) is made, so that if the -15V supply drops below -13.5V, IC5/1 and VT2 clamp the analogue sample capacitors to 0V to inhibit outputting and protect the demultiplexers. A RESET signal via VT1 also resets the capacitors.

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DUET desk : 60 LED mimic card : functional block diagram	2.8.1
DUET desk : 120 LED mimic card : functional block diagram	2.8.2

General

1. LED mimic cards are an option which, when installed, display by re illumination below a channel number those channels that are 'on' (i.e. at greater than 1%) in the selected playback (A,B or T) or at the output (). In addition any channel under control of the channel control section will cause its LED to blink, if the mimic is on. The mimic can also be switched by the view pushes (?) to temporarily display the contents of the playback store or memory.

2. The LED card comes in two types, 60 or 120 channel. For other channel capacities, some LED's are covered by the bezel. The card is mounted inside the desk behind the perspex bezel which show the channel numbers.

3. Description of the LED mimic cards is made with reference to the functional block diagrams (fig. 2.8.1, 2.8.2) and the circuit diagrams

Detailed description, 60 way

4. Incoming channel bus data (CHN⁰ - CHN⁶ and CHN ON) is latched by the strobe signal CHN STB (IC17,18). CHN STB signals, at its leading edge, that the channel number and on/off data is now correct but will change to the next channel in 2uS. Data input latching is timed by C13, R109.

5. Four channels of mimic data are stored in IC11,13 following decode of CHN⁰ and 1 by IC15. Each time CHN⁰ and 1 are both 0 latched into a different one of 15 4-bit latches, defined by a decode of CHN² - CHN⁶ (IC12,14,16).

6. IC14 and IC16 do a 4 to 16 line decode of CHN² to CHN⁵ (with CHN⁵ applied through IC12) selecting either IC14 or IC16. CHN⁶ defines the upper limit of operation at IC12 whilst a third input representing every fourth count (para 5) is also applied. C9, R77 provide the timing for the data output latching.

Detailed description, 124 way

7. Incoming bus data (CHN₀ - CHN₆ and ON) is latched by the strobe signal CHN STB (IC36, 38). Decode organisation is centred around a PROM (IC37) which decodes the channel number address to row and column address which follow the same structure as the LED configuration, i.e. 4 rows of 30 columns.
8. Timing sequence for the decode is established by two monostables of 2 μ S and 20 μ S (IC35) which, operating serially, define (firstly) row operation then column operation. The PROM contains column drive information in one half and row drive in the other half, the two halves being addressed sequentially as defined by the timing sequence line which controls A6 address input.
9. Row decode from the PROM is provided by data lines D₀ and D₁ which are clocked into two bistable latches (IC31). A three line to eight line selection is achieved by IC34 to provide appropriate row ON drive via VT121 - VT124 when CHN ON is set and row OFF drive (four alternate lines) when CHN ON is clear. The ON and OFF drives are then diode gated onto the selected bit input (row) of all the 4-bit latches driving the LED's, prior to the appropriate column being clocked by the column decode. The other bits in the latch are left as set by their feedback resistors setting their D inputs.
10. Column decode data from the PROM has the CHN₀ (latched) input added to it to provide a 32 line decode, the last two of which are unused. This is achieved by four 3 line to 8 line decoders (IC39 - 42) decoding PROM bits D₁ and D₀ together with CHN₀ and decoder selection being done by 2 line to 4 line decoding of PROM bits D₂ and D₃ (IC32). The 30 column drive lines each clock four latches.
11. The mimic data latches are thus the focal point of a 30 x 4 matrix. When set, the latch outputs light their particular LEDs through transistor drive stages.

Sect 2 Chap 9

FRONT PANEL :

PANEL MOTHERBOARD AND OTHER ITEMS
(1606, 1609, 1610, 1611)

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Fig.

DUET desk : front panel motherboard and other
items : block diagram

1

General

1. This chapter deals with all those controls and displays which are visible when viewing DUET from the front. Most of these items are mounted on the front panel motherboard and appear through apertures in the desk front. Others are independent of the front panel motherboard mechanically, but have their electrical connections to the system made through it. The numerical indicators are likewise independent of the front panel motherboard, being mounted on their own small printed cards which are electrically connected straight to the processor motherboard.

2. Description of the front panel items is made with reference to the block diagram, fig. 2.9.1 and to the various circuit diagrams.

Detailed description

3. Functional description of front panel items is included in Sect. 2 Chap. 2 which shows how the control and display functions interface to the microprocessor. The PROGRAM section describes how controls and displays affect the program. The description here is limited to the controls and displays themselves.

4. Push switches SW1, SW5 to SW43, together with the programming 8 way dual-in-line switch SW2 and the fade-time switch SW4 are all contained within an address encoding diode matrix. Selection addressing of the matrix is done by CON C₅ to CON C₆ and the encoded selection is output on the CON D₀ to CON D₇ lines. Most of the push switches contain lamps which are lit by program control. The fade-time switch has two associated LED mimics for the minutes and seconds settings while a warning LED indicates an invalid memory. These LEDs are on a small printed cards which connect to PL4 and PL8 on the front panel motherboard. The channel meter is mounted on the front panel motherboard.

5. The four faders; A/B up, A/B down, T and output (grand master) are all separately mounted items which connect respectively to PL7, PL6, PL5 and PL3 on the front panel motherboard. The wheel assembly is similarly mounted. It contains a drive which turns a regularly-slotted disc, the slots providing optical encoding for two light emitter/receiver devices. The positioning of the two optical encoders is critical, as the square wave output of the first must be 90° in advance of the second (Sect. 2 Chap. 2). The wheel information connects the front panel motherboard through PL9.

6. Numeric displays are of the seven segment type with the first digit of the channel/memory indicator being solely a 1 with + or - options, and all three digits having decimal point options. Drive to the 0-9 digits is in binary coded decimal form, the coding for each figure providing the drive to illuminate the appropriate segments. Both numeric displays are mounted on their own printed circuit card which connects directly to the processor motherboard.

Se(: 2 Chap. 10 POWER SUPPLY UNIT & LAMP REGULATOR (1333)

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General

1. The power supply for DUET is housed in a sub chassis at the back left of the desk. It consists of a power supply unit manufactured by Gould which delivers the DUET requirements of +5V, +15V and -15V from a mains input. The unit is a type MGT 5-20 for 220V - 240V operation or a type MGT 5-20A for 110V - 120V operation.

2. Lamp supply is produced by a lamp regulator card which is push-fitted to the chassis at the rear in such a way that four LED supply monitors (+15V, -15V, +5V, +LPS) and a lamp supply adjuster show through the chassis and out of the rear of the desk.

3. Description of the power supply is made with reference to the circuit diagrams of the power supply and the regulator card.

Detailed description

4. The Gould power supply unit is separately fused at 3.15A (for 220V) or 6.3A (for 110V). Mains input is neon monitored between the line and neutral and its three outputs are LED monitored on the lamp regulator card. For further details of this unit, the manufacturers information should be consulted - APPENDIX section.

5. The lamp regulator card uses and monitors (LED 2,3,4) the +5V, +15V and -15V delivered by the power supply unit. The lamp intensity control (RV1) is part of a resistive path between +5V and 0V and it applies a voltage between 2V and 4.5V to the inverting input of an operational amplifier, IC1. IC1 is slow to react to changes of input due to associated input resistor R10 and feedback capacitor C5. This ensures loop stability.

6. The following transistor stages (VT1 - VT4) driven by IC1 can be regarded as a unity gain amplifier providing current limiting between 3A and 5A for voltages between +2V and +4.5V when delivering the +LPS output. The output is feedback to the non inverting input of the operational amplifier to establish the regulation loop.