Introduction

CD80 Pack Electronics Repair Procedures

This section provides information on manual organization, details procedures for getting your suggestions to Strand Lighting and receiving help if necessary, and shows the equipment required for CD80 Pack electronics repair.

1. ABOUT THIS MANUAL

This manual provides information on the operating and maintenance procedures for CD80 2.4Kw, 6.0Kw, and 12.0Kw Packs. Circuit descriptions are included in the CD80 Pack Repair Procedures Manual for those who wish to do their own circuit level maintenance of this equipment. 1.2Kw dimmer packs use different electronics, and are discussed in separate publications.

1.1 Manual Organization

This manual contains 5 major sections as shown below.

INTRODUCTION

Manual organization (chapter 1)
How to get help (chapter 2)
Equipment Required (chapter 3)

MULTIPLEX CONTROL MODULE

Circuit Description (chapter 4)
Trouble-shooting And Calibration (chapter 5)

ANALOG CONTROL MODULE

Circuit Description (chapter 6)
Trouble-shooting And Calibration (chapter 7)

3.2 *Other Equipment Required*

One "Known Good" CD80 Rack Control Module

3 1/2 Digital Multi-Meter

Oscilloscope

The oscilloscope should have a bandwidth of at least 20MHz. A dual trace oscilloscope will allow simultaneous display of waveforms from the Ramp Card under test and the Reference Ramp Card, but is not a necessity.

A.C. Regulation

During the calibration process, it is important that the AC line be stable (+/- 1 volt). The end user must supply a stable AC line source. A variac transformer and voltmeter will allow adequate manual adjustments for long term variations in the AC line.

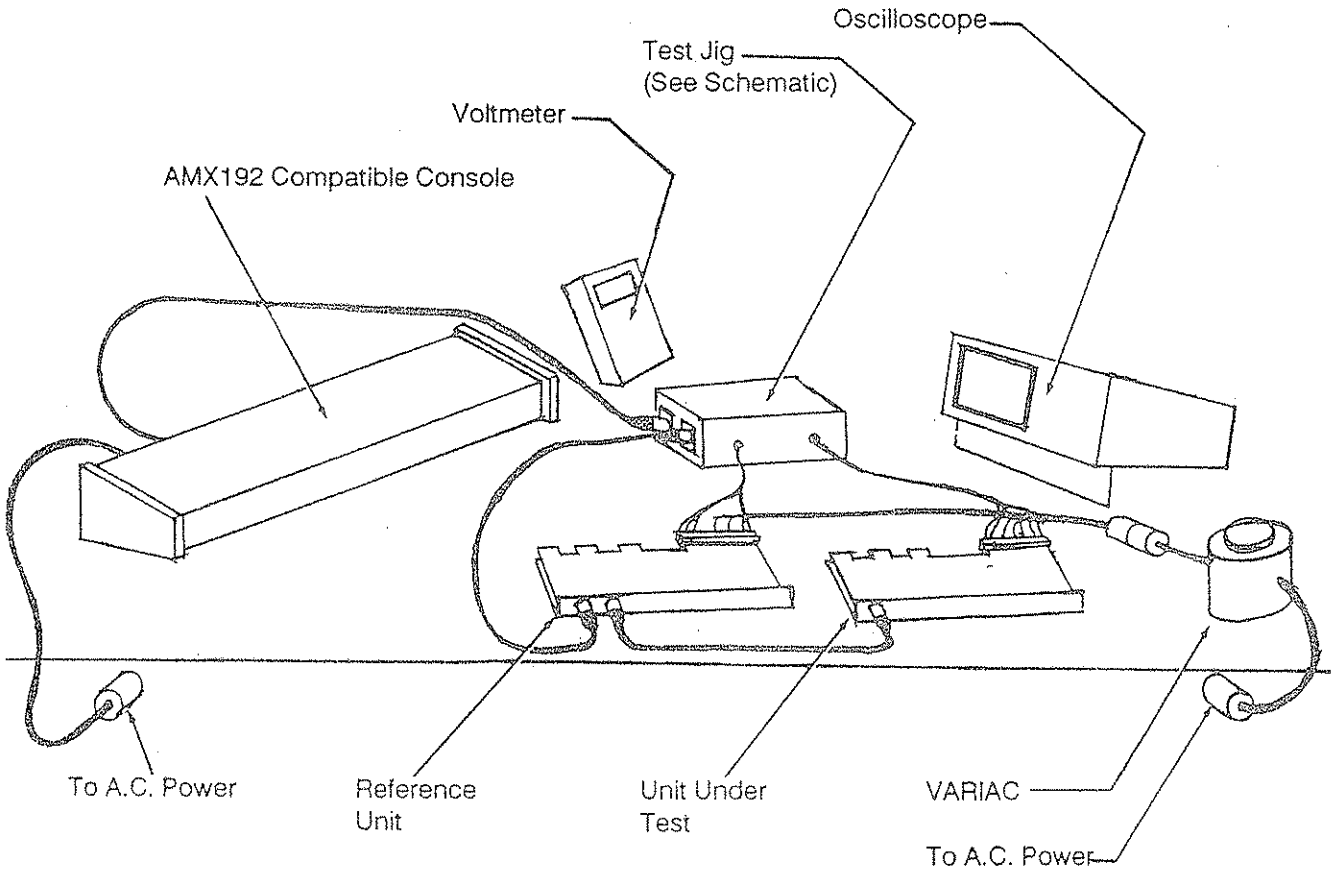

Figure 2. Control Module Test Setup

2. TECHNICAL ASSISTANCE

CD80 Packs are designed to require a minimum of maintenance and servicing. Circuit descriptions are included in this manual for those who wish to to do all of their their own repair and maintenance work. Basic Trouble-shooting for the CD80 Pack as a whole is detailed in the CD80 Pack Operator's Reference. 1.2Kw Packs use different electronics, and are discussed in separate publications. Other documentation may be purchased through Strand Lighting Customer Service.

2.1 *In Case Of Problems*

If equipment fails to operate properly upon installation, or under normal load and temperature conditions, and basic trouble-shooting procedures are not effective, please contact Strand Lighting Field Service at the office serving your area. Strand Lighting will issue an RGA (Return Goods Authorization) before the return of any defective materials. This allows tracking of returned equipment, and speeds its return to you.

2.2 *Technical Questions*

For technical questions regarding setup, operation, or maintenance of this equipment, please contact the Strand Lighting Field Service office serving your area (see reverse side of manual title sheet for addresses and phone numbers).

2.3 *Parts Purchases*

For purchase of spare parts or documentation, Please contact Strand Lighting Customer Service in the Rancho Dominguez office.

2.4 *Comments and Suggestions*

For comments regarding equipment functions and/or suggested enhancements, please call or write to the Control and Dimming Product Manager at the Rancho Dominguez office.

For comments on this manual, please write to the Technical Publications Manager at the Rancho Dominguez office.

3. EQUIPMENT REQUIRED

3.1 Test Jig

The dimmer Control Module can be repaired by using the test jig illustrated below. This test jig is not available as a standard part from Strand Lighting, but is relatively easy to construct. Trouble-shooting is accomplished by comparison of the defective unit with a known good Control Module.

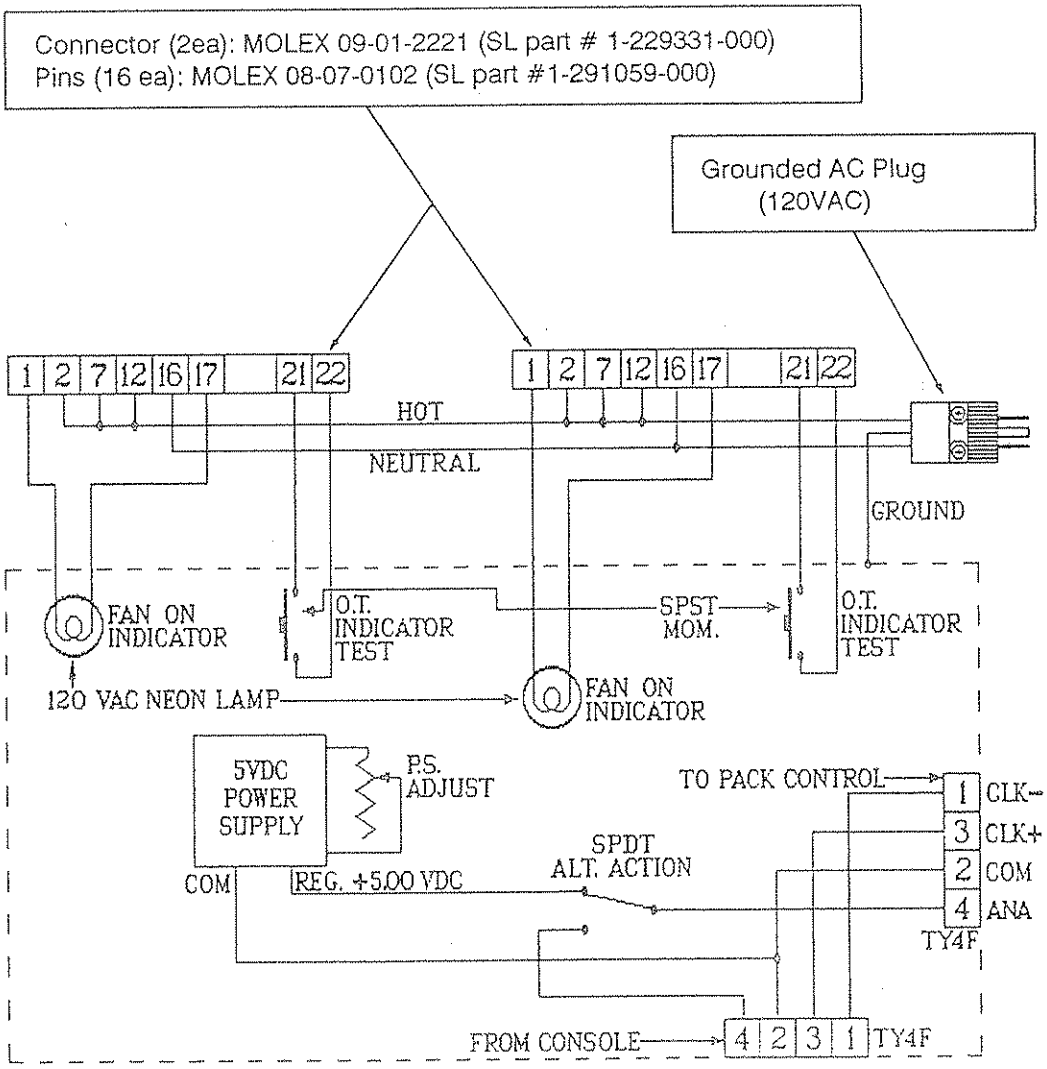

Figure 1. Control Module Test Jig Schematic

Multiplex Control Module

CD80 Pack Electronics Repair Procedures

This section provides circuit descriptions and information on trouble-shooting and calibration of the CD80 Pack Multiplex Control Module.

4. MULTIPLEX CONTROL CIRCUIT DESCRIPTION

The Multiplexed Control Module (part #3-258358-010) is the standard Control Module provided with CD80 Packs. Dimmer packs using this Control Module may be controlled by any Strand Lighting multiplexed output control console (Mantrix, MiniPalette, Light Palette, etc.), or any other signal source conforming to the USITT AMX192 Analog Multiplex Dimmer Control standard. Contrary to some usage, this is not a digital dimmer, but uses a time domain multiplexed analog control signal of 0 to +5VDC.

The Control PCB schematic (13-722783-010) should be referenced for the following discussions. For purposes of discussion, we will divide the Control Module into a Power Supply Section and a Ramp/Demultiplexing Section.

4.1 *Power Supply*

The Power Supply circuitry supplies regulated DC, fault shutdown control circuitry, AC reference supplies, and system fault status indicators. It can be roughly divided into 3 sections, which are:

A. Power Control and Status
B. Power Supply
C. Voltage Reference Sources

A. Power Control and Status

SCR1 applies AC power to the Regulated DC Power Supply and the fan (thus energizing the Control Module) when the following conditions are met:

1) The clock signal is present on gate 1A pin 12.
2) The thermostat is "open" (no overtemp condition).
3) Correct input AC voltage is present.

1) Clock Sensing and Shutdown

Clock sensing is with the presence of positive clock pulses on pin 12 of IC 1A. These pulses immediately discharge C4 to ground via D30, causing pin 12 of IC 1A to go high. This turns on SCR1 via Q1 and Q2 (thus energizing the Regulated DC Power Supply and fan) as long as the other conditions are met. If the clock is lost for any reason, C4 is slowly discharged via R9 to B+, and causes pin 10 of IC 1A to switch to ground. This takes about 1/2 second. The base drive signals to Q1 and Q2 are thus removed, and SCR1 is de-energized.

2) Overtemperature Sensing and Shutdown

Over-temperature indication on I2 is obtained from thermostat closure, which energizes the collector of Q5 and turns on the overtemp indicator I2. This simultaneously applies B+ to diode D29, which shuts down the base drive to Q1. The regulator is then de-energized as SCR1 is turned OFF.

Since this shuts down the Regulated DC Power Supply, the oscillator which outputs from pin 4 of IC1A is activated. This causes transistor Q4 to be switched on and off, thus flashing I3 (the power indicator LED) On and OFF. When Q4 is ON, the emitter of Q5 is grounded, causing the overtemp indicator light to go OFF. This causes the overtemp and power indicator lights to flash alternatively on an overtemp condition.

3) Correct Voltage on the AC input

Power indicator driver Q4 obtains its base input voltage from pin 4 of IC1A. This provides a flashing output if the voltage from regulator 2A drops below 4.00VDC. This condition is caused by undervoltage on phase A, or by SSR1 being shut down by overvoltage or overtemperature conditions.

An overvoltage primary condition also causes indicator I1 to flash by applying a neon ionization breakdown voltage to the summing junction of D11, D12, and D13 when the primary center tap(s) of T1, T4, or T5 reach approximately 70VAC RMS. At that point, neon overvoltage indicator I1 flashes in a "relaxation oscillator" mode as its shunt capacitor C70 charges and discharges.

All power transformers except T2 are rated at 240VAC RMS on their primary side, and are capable of indefinitely sustaining this input without damage. Only T2 is connected as a 120VAC rated unit, and is shut down via Q1/SCR1 when a fault is sensed.

In cases where an overvoltage exists on phase A, Zener diode D32 is driven into conduction. This shifts the base bias voltage of transistor Q6 to negative, and turns it off. Once Q6 is no longer conducting, the voltage at the emitter jumps to the "Clock Driver DC" voltage (approx. 10.5VDC), thus shutting down Q1, Q2, and SCR1 and turning the Control Module off.

B. DC Power Supply

Regulated DC power for the Control Module is provided by a Regulated DC Power Supply consisting of transformer T2, Diodes D1-D4, voltage regulator IC2A, and associated circuitry. This power supply is protected by the circuitry described above, and feeds all control circuitry except the incoming clock receiver chip (IC6F) and parts of the indicator shut-down circuitry as indicated above.

Power for the additional circuitry is provided by a transistor regulator consisting of Q3, R19, C73, and D10, with zener diode D10 being the reference. This supply is used to power the input clock receiver, the overtemp indicator oscillator, and the overvoltage shutdown transistor.

C. Phase A, B, and C Voltage Sources

Transformers T3, T4, and T5 are identical reference transformers, and are supplied from Phase A, B, and C respectively.

Each secondary output reference is adjusted to provide full output of each SSR driver when two conditions are met:

1) The line voltage is the specified voltage for the system (100VAC, 120VAC or 220VAC RMS).
2) The analog signals are set to full (5.00VDC)

Adjustment of each phase reference is done via ramp adjustment potentiometers R64, R104, and R105.

4.2 Ramp/Demultiplexing Circuit

The Control Module input signal consists of 192 analog multiplexed voltage levels, associated timing clock, and full-wave, rectified reference signals from each input phase. The Ramp/Demultiplexing circuit demultiplexes the input analog signals in such a fashion as to select the correct analog levels to control twelve solid state relays (SSRs) with the correct phase-firing information. The Ramp/Demultiplexing section is composed of seven building blocks:

A. Clock Receiver and Reset Detector
B. Counter/Decoder Block
C. Analog Buffer
D. Analog Demultiplexer
E. AC Zero Crossover Detector
F. Square Law Curve Generator
G. Output Solid State Relay Driver

A. Clock Receiver and Reset Detector

The Clock Receiver and Reset Detector separates the reset pulse from the remainder of the clock pulse train and delays the clock signal. The clock signal is received by 6F, an LM311N analog comparator. The positive clock signals are modified by a NAND gate one-shot on IC 6E, which operates on all positive inflections and converts these signals to negative pulses 27 microseconds wide. A second one-shot operates on the test point "C" positive-going signal, and converts the positive transition to a negative-going pulse 7 microseconds wide (i.e., the clock pulse is delayed and inverted at test point "D"). The start pulse of the incoming clock signal is 40 microseconds wide, while all other clock pulses are 8 microseconds wide. Reset at start-of-cycle is achieved by NANDing the clock (test point "A") with a modified clock (test point "C"), delaying this signal by 1 microsecond, and inverting the signal. This results in a RESET (positive) pulse approximately 12 microseconds wide applied to all counters.

B. Counter/Decoding Circuit

The Counter/Decoding circuit consists of IC 3C, 3D, 4A, 4B, 4C, and 4D.

Analog information is decoded and transferred to the proper analog storage capacitor when two conditions are met at IC 3C and IC 3D:

1) The proper binary inputs are present
2) A "Zero" input level is present at the proper Demultiplexer Inhibit input (pin 6).

IC 4A is a dual four-bit counter, one half of which counts "0-11" and is then reset via the logic circuitry terminating at IC 11A pin 7. The twelve-pulse (serial) train is then converted to four-bit parallel binary control signals applied to the demultiplexers 3C and 3D (pins 9, 10, and 11).

Counter 3C accepts counts "0-7" and counter 12B provides a count of "8-11" as controlled by the "overflow" status of IC4C, pin 6. Demultiplexer 3C thus operates in tandem with 3D once the latter obtains its maximum control signal count of "7" and IC 11A pin 6 goes high.

Decoding of dimmer counts higher than "12" (corresponding to Dimmer Pack identities 2 through 16) is obtained by virtue of a delaying signal derived from an octal (Johnson) counter (IC 4A) which provides an enabling gate whose width is 12 clock pulses wide and whose delay is a function of the output stage tap utilized by switch SW1.

The octal counter receives one pulse for each count of 12 out of the four-bit counter. A time-delayed enabling window, 12 clock pulses wide, is provided as a function of the "group selection" switch (SW1).

Since the group selector switch and Johnson counter normally accommodates only eight groups for a total of 96 dimmers, an additional provision is made to count from pulse "97-192" by inhibiting demul-

tiplexers 3D and 3C during the initial count of "96", by using the "C0" function of the Johnson counter coupled to a "divide by two" output of the previously unused section of IC 4C.

The "97-192" count enabling function thus occurs when the binary counter at IC 4C pin 11 is at zero, and SW2 is at position B. The enabling gate so obtained is also 96 pulses long, but delayed from the first pulse by a time period 96 pulses long.

For the simplest decoding case (counts "0-11"), the counter/decoding circuit decodes the clock signals in such a fashion as to cause IC 3D to store analog signal information upon the driver storage capacitors as follows: Clock "0" and clock "1" cause analog information to be stored on C28 first, and C26 second. C24 and C22 respectively have clock pulses stored during clock pulses "3" and "4", etc. The clock decoding and analog demultiplexing is repeated until all 12 capacitors have analog signal levels stored on them.

All counters are reset by the Start-of-Cycle reset pulse ("CLR") on the card.

C. Analog Buffer

The Analog Buffer (IC 5C) has a unity gain, a high input impedance, and a very low output impedance. The prime function of this circuit block is to transfer the analog input signal to the Analog Demultiplexing Circuit (IC 3C, and IC 3D) without loading the input analog line.

D. Analog Demultiplexer

Analog demultiplexing is provided by IC 3C, IC 3D, and capacitors C17 through C28, which permit analog signal levels to be demultiplexed and stored. The input analog signals are transferred from test point "L" to pin 3 of both IC 3C and IC 3D. The capacitor to which a particular analog signal is transferred is determined by the binary digital number on pins 11, 10, 9, and 5 of IC 3C and IC 3D. The binary digital number is developed by the Counter/Decoding circuit. The correct time period and sample storage time are determined by the signal "logic Zero" on pin 6 of IC 3C or IC 3D. The sample storage pulse width and timing are developed by the Clock Receiver and Reset Detector Circuit.

E. AC Zero Crossover Detector

The AC Zero Crossover Detector (one for each power input phase) detects power line zero crossover (5 degrees +/- 2 degrees from zero volts). Input to this circuit is negative full-wave rectified 15VAC RMS (transformed line voltage) from the Power Supply section. Q7 operates on this signal and outputs a negative pulse to a negative NAND gate edge detector (IC 6D). This pulse is shaped and inverted (test point "H") and utilized in the sample-and-hold section of the Square Law Curve Generator (IC 6C). IC 6D also has a negative edge transition detector that is used to reset the reset integrator of the Square Law Curve Generator (test point "I").

F. Square Law Curve Generator

The Square Law Curve Generator (one for each input power phase) develops a 60HZ based non-linear ramp reference signal applied to the negative input of all of the output drivers (IC 2B, 2C, 2D, 2E, 2F, 2G). The shape of the reference signal then determines the relationship of analog input signal level to the pulse width output of each driver (and thus the AC output of each dimmer).

For simplicity, the following description is based on the phase A circuitry. Circuitry for phase B and C is identical except for the component designations.

The heart of the Square Law Curve Generator is a reset integrator with one input voltage "gain" change. The gain change is accomplished with a Zener diode D47 in series with the full-wave signal from transformer T3. The most positive voltage output from Reset Integrator 5C is sampled and stored on C37 on a half-cycle by half-cycle basis. The Reset Integrator is reset to zero at the end of each half-cycle of the AC power line. The voltage stored on C37 is translated and referenced to ground with differential amplifier 5B, which inverts the C15 voltage with a gain of 1.0. This voltage is summed with the integrator output and delivered to test point "J".

G. Output Solid State Switch Driver

The Output Solid State Switch Driver outputs a 6.5V signal minimum into a nominal 1.5 Kohm load. The positive input signal to drive the output driver comes from the charge stored on each capacitor (.01 uF) connected to their respective inputs. The voltage input at this point is 0 to +5VDC. If an oscilloscope probe is used to measure the charge of the capacitor, the 10 megohm input impedance of the scope probe will discharge the capacitor and large error signals will appear. The signal existing on the negative input of the Solid State Switch Driver comes from the Square Law Curve Generator. A logic one (6.5V or more) exists at the output of the Solid State Switch Driver whenever the positive input signal is more positive than the negative input signal.

5. MULTIPLEX CONTROL TEST & CALIBRATION

5.1 Basic Trouble-Shooting

The dimmer Control Module can be repaired by using the test jig illustrated on page 8 and 7 . Trouble-shooting is accomplished by comparison of the defective unit with a known good Control Module.

A. Plug a known good Module into one of the MOLEX connectors and the defective Module into the other MOLEX connector. Place both Modules on the work bench with the circuit side up for access with the oscilloscope probe (see page 8).

B. Plug the AC connector into an AC outlet (100VAC, 120VAC, or 220VAC as appropriate).

C. Check for functioning of each ramp circuit. Oscilloscope should show a ramp (reverse "S" curve) which starts at +5VDC and goes down to about .2VDC. This ramp is not linear. If the ramp circuit for any of the 3 phases is defective, repair it before to proceeding.

D. Once all ramp circuits are functional, plug the output from a Strand Lighting multiplexed control console (or other device which outputs a USITT Standard AMX192 control signal) into the test jig. Plug the test jig output into one of the Control Modules and connect the two together using a daisy chain control cable.

E. The "Fan Indicator" on the test jig should light up. If not, trouble-shoot the clock detection circuit and repair the fan turn-on.

F. Check the over-temperature circuit by pushing the O.T. test button.

G. Patch 12 dimmers at a time into the 12-channel Mantrix (or otherwise address successive groups of 12). Check the Module with the "Rack Select" switch in both the "A" and "B" positions and with the thumbwheel switch in position "1-8". If the system works properly with some thumbwheel setting, but not others, the counter/decoder section is defective.

5.2 Calibration

Calibration of the Control Module is accomplished by observation of the output to the SSR Module under controlled conditions. This procedure must be done with the correct frequency power applied to the Module (i.e., 50Hz or 60Hz).

A. Connect the AC input of the fixture to a Variac and monitor the line voltage on phase A.

B. Set phase A voltage to specification voltage +/- 0.5V RMS (100VAC, 120VAC, or 220VAC).

C. Select +5V on the analog input switch of the test jig. This puts a calibrated +5VDC into the analog buffer of the CD80 Pack Control Module.

D. Set the Control Module "single-phase/3-phase" switch to single-phase ("1ϕ").

E. Verify that the incoming signal level is 5.00V +/- .05VDC. Adjust as necessary.

F. Monitor dimmer driver outputs 7, 8, 9, 10, 11, and 12 on the oscilloscope while adjusting trim pot R105. Verify that this adjusts all 6 of these dimmers, and that adjustment can be made to produce a 100% duty cycle signal on these dimmers.

G. Switch the "single-phase/3-phase" switch on the Control Module to 3-phase ("3ϕ") and verify that only dimmers 9, 10, 11, and 12 are affected by trim pot R105.

H. Adjust driver outputs 1-4 with trim pot R103 to barely produce 100% duty cycle. To do this, watch the oscilloscope until the downward-going pulse just disappears. Then add 1/4 turn in the increasing output direction.

I. Adjust driver outputs 5-8 with trim pot R104 for 100% duty cycle output, adding 1/4 turn in the same manner.

J. Adjust driver outputs 9-12 with trim pot R105 for 100% duty cycle output, adding 1/4 turn in the same manner.

K. Verify that all driver outputs provide a minimum of 6.5VDC output with maximum control input to the card.

L. Verify that all outputs provide zero output (no pulses observed on the scope) with the control signals returned to zero.

M. Seal all potentiometers with Glyptol or other suitable means.

Analog Control Module

CD80 Pack Electronics Repair Procedures

This section provides circuit descriptions and information on trouble-shooting and calibration of the CD80 Pack Analog Control Module.

6. ANALOG CONTROL CIRCUIT DESCRIPTION

An Analog Control Module (P/N 3-258362-010) is available which allows a CD80 Pack to be controlled by 12 discreet, DC analog input signals rather than the standard multiplexed analog signal. If these discreet signals are from a console which uses a pulse-width modulated dipless crossfader, it is necessary to provide input filtering in a separate outboard box. This is available from Strand Lighting in a custom Splitter Box.

The Control PCB schematic (13-722783-010) should be referenced for the following discussions. For purposes of discussion, we will divide the Control Module into a Power Supply Section and a Ramp/Demultiplexing Section.

6.1 *Power Supply*

The Power Supply circuitry supplies regulated DC, fault shutdown control circuitry, AC reference supplies, and system fault status indicators. It can be roughly divided into 3 sections, which are:

A. Power Control and Status
B. Power Supply
C. Voltage Reference Sources

A. Power Control and Status

SCR1 applies AC power to the Regulated DC Power Supply and the fan (thus energizing the Control Module) when the following conditions are met:

1) Power is applied to the circuit.
2) The thermostat is "open" (no overtemp condition).
3) Correct input AC voltage is present.

1) Clock Sensing and Shutdown

Clock sensing is bypassed in the discreet analog version of the Control Module by a jumper which connects the "Clock Driver DC" signal at R73 to the pin 13 input of IC1A. This forces the output at IC1A pin 11 high, which turns on SCR1 via Q1 and Q2 (thus energizing the Regulated DC Power Supply and fan) as long as the other conditions are met. If phase A is removed, this circuit will shut the Control Module OFF.

If the clock is lost for any reason, C4 is slowly discharged via R9 to B+, and causes pin 10 of IC 1A to switch to ground. This takes about 1/2 second. The base drive signals to Q1 and Q2 are thus removed, and SCR1 is de-energized.

2) Overtemperature Sensing and Shutdown

Over-temperature indication on I2 is obtained from thermostat closure, which energizes the collector of Q5 and turns on the overtemp indicator I2. This simultaneously applies B+ to diode D29, which shuts down the base drive to Q1. The regulator is then de-energized as SCR1 is turned OFF.

Since this shuts down the Regulated DC Power Supply, the oscillator which outputs from pin 4 of IC1A is activated. This causes transistor Q4 to be switched on and off, thus flashing I3 (the power indicator LED) On and OFF. When Q4 is ON, the emitter of Q5 is grounded, causing the overtemp indicator light to go OFF. This causes the overtemp and power indicator lights to flash alternatively on an overtemp condition.

3) Correct Voltage on the AC input

Power indicator driver Q4 obtains its base input voltage from pin 4 of IC1A. This provides a flashing output if the voltage from regulator 2A drops below 4.00VDC. This condition is caused by undervoltage on phase A, or by SSR1 being shut down by overvoltage or overtemperature conditions.

An overvoltage primary condition also causes indicator I1 to flash by applying a neon ionization breakdown voltage to the summing junction of D11, D12, and D13 when the primary center tap(s) of T1, T4, or T5 reach approximately 70VAC RMS. At that point, neon overvoltage indicator I1 flashes in a "relaxation oscillator" mode as its shunt capacitor C70 charges and discharges.

All power transformers except T2 are rated at 240VAC RMS on their primary side, and are capable of indefinitely sustaining this input without damage. Only T2 is connected as a 120VAC rated unit, and is shut down via Q1/SCR1 when a fault is sensed.

In cases where an overvoltage exists on phase A, Zener diode D32 is driven into conduction. This shifts the base bias voltage of transistor Q6 to negative, and turns it off. Once Q6 is no longer conducting, the voltage at the emitter jumps to the "Clock Driver DC" voltage (approx. 10.5VDC), thus shutting down Q1, Q2, and SCR1 and turning the Control Module off.

B. DC Power Supply

Regulated DC power for the Control Module is provided by a Regulated DC Power Supply consisting of transformer T2, Diodes D1-D4, voltage regulator IC2A, and associated circuitry. This power supply is protected by the circuitry described above, and feeds all control circuitry except the incoming clock receiver chip (IC6F) and parts of the indicator shut-down circuitry as indicated above.

Power for the additional circuitry is provided by a transistor regulator consisting of Q3, R19, C73, and D10, with zener diode D10 being the reference. This supply is used to power the overtemp indicator oscillator and the overvoltage shutdown transistor.

C. Phase A, B, and C Voltage Sources

Transformers T3, T4, and T5 are identical reference transformers, and are supplied from Phase A, B, and C respectively.

Each secondary output reference is adjusted to provide full output of each SSR driver when two conditions are met:

1) The line voltage is the specified voltage for the system (100VAC, 120VAC or 220VAC RMS).
2) The analog signals are set to full (5.00VDC)

Adjustment of each phase reference is done via ramp adjustment potentiometers R64, R104, and R105.

6.2 Ramp/Driver Circuit Description

The Analog Control Module input signal consists of 12 analog voltage levels and full-wave, rectified reference signals from each input phase. The Ramp/Driver circuitry allows the analog levels to control twelve solid state relays (SSRs) with the correct phase firing information. Circuitry involved in the demultiplexing of the AMX192 signal is not removed from the PCB when it is modified for discreet analog use. However, the two types of input cannot be used simultaneously due to the differences in the basic analog signals used. Since the demultiplexing section is not used in this configuration, it is not discussed here. The Ramp/Driver section is composed of three basic building blocks:

A. AC Zero Crossover Detector
B. Square Law Curve Generator
C. Output Solid State Relay Driver

A. AC Zero Crossover Detector

The AC Zero Crossover Detector (one for each power input phase) detects power line zero crossover (5 degrees +/- 2 degrees from zero volts). Input to this circuit is negative full-wave rectified 15VAC RMS (transformed line voltage) from the Power Supply section. Q7 operates on this signal and outputs a negative pulse to a negative NAND gate edge detector (IC 6D). This pulse is shaped and inverted (test point "H") and utilized in the sample-and-hold section of the Square Law Curve Generator (IC 6C). IC 6D also has a negative edge transition detector that is used to reset the reset integrator of the Square Law Curve Generator (test point "I").

B. Square Law Curve Generator

The Square Law Curve Generator (one for each input power phase) develops a 60HZ based non-linear ramp reference signal applied to the negative input of all of the output drivers (IC 2B, 2C, 2D, 2E, 2F, 2G). The shape of the reference signal then determines the relationship of analog input signal level to the pulse width output of each driver (and thus the AC output of each dimmer).

For simplicity, the following description is based on the phase A circuitry. circuitry for phase B and C is identical except for the component designations.

The heart of the Square Law Curve Generator is a reset integrator with one input voltage "gain" change. The gain change is accomplished with a Zener diode D47 in series with the full-wave signal from transformer T3. The most positive voltage output from Reset Integrator 5C is sampled and stored on C37 on a half-cycle by half-cycle basis. The Reset Integrator is reset to zero at the end of each half-cycle of the AC power line. The voltage stored on C37 is translated and referenced to ground with differential amplifier 5B, which inverts the C15 voltage with a gain of 1.0. This voltage is summed with the integrator output and delivered to test point "J".

C. Output Solid State Switch Driver

The Output Solid State Switch Driver outputs a 6.5V signal minimum into a nominal 1.5 Kohm load. The positive input signal to drive the output driver comes from the charge stored on each capacitor (.01 uF) connected to their respective inputs. The capacitor is charged from a 0 to +10VDC discreet analog signal which is input through a voltage divider to present a 0 to +5VDC signal at the sample and hold capacitor. The signal on the negative input of the Solid State Switch Driver comes from the Square Law Curve Generator. A logic one (6.5V or more) exists at the output of the Solid State Switch Driver whenever the positive input signal is more positive than the negative input signal.

7. ANALOG CONTROL TEST & CALIBRATION

7.1 Basic Trouble-Shooting

The dimmer Control Module can be repaired by using the test jig illustrated on page 8 and page 7 . Trouble-shooting is accomplished by comparison of the defective unit with a known good Control Module.

A. Plug a known good Module into one of the MOLEX connectors and the defective Module into the other MOLEX connector. Place both Modules on the work bench with the circuit side up for access with the oscilloscope probe (see page 8).

B. Plug the AC connector into an AC outlet (100VAC, 120VAC, or 220VAC as appropriate).

C. Check for functioning of each ramp circuit. Oscilloscope should show a ramp (reverse "S" curve) which starts at +5VDC and goes down to about .2VDC. This ramp is not linear. If the ramp circuit for any of the 3 phases is defective, repair it before to proceeding.

D. Once all ramp circuits are functional, plug the output from a Strand Lighting multiplexed control console (or other device which outputs a USITT Standard AMX192 control signal) into the test jig. Plug the test jig output into one of the Control Modules and connect the two together using a daisy chain control cable.

E. The "Fan Indicator" on the test jig should light up. If not, trouble-shoot the clock detection circuit and repair the fan turn-on.

F. Check the over-temperature circuit by pushing the O.T. test button.

7.2 Calibration

Calibration of the Control Module is accomplished by observation of the output to the SSR Module under controlled conditions. This procedure must be done with the correct frequency power applied to the Module (i.e., 50Hz or 60Hz).

A. Connect the AC input of the fixture to a Variac and monitor the line voltage on phase A.

B. Set phase A voltage to specification voltage +/- 0.5V RMS (100VAC, 120VAC, or 220VAC).

C. Make sure that the voltage coming in to each of the analog inputs is +10VDC. This can be done by making an adapter with a 10VDC power supply which plugs directly into the discreet analog input plug.

D. Set the Control Module "single-phase/3-phase" switch to single-phase ("1ϕ").

E. If calibrating an Analog Control Module, verify that all of the the incoming analog voltages are +10.00 +/- .05VDC. If not, the console being used may need adjustment

F. Monitor dimmer driver outputs 7, 8, 9, 10, 11, and 12 on the oscilloscope while adjusting trim pot R105. Verify that this adjusts all 6 of these dimmers, and that adjustment can be made to produce a 100% duty cycle signal on these dimmers.

G. Switch the "single-phase/3-phase" switch on the Control Module to 3-phase ("3ϕ") and verify that only dimmers 9, 10, 11, and 12 are affected by trim pot R105.

H. Adjust driver outputs 1-4 with trim pot R103 to barely produce 100% duty cycle. To do this, watch the oscilloscope until the downward-going pulse just disappears. Then add 1/4 turn in the increasing output direction.

I. Adjust driver outputs 5-8 with trim pot R104 for 100% duty cycle output, adding 1/4 turn in the same manner.

J. Adjust driver outputs 9-12 with trim pot R105 for 100% duty cycle output, adding 1/4 turn in the same manner.

K. Verify that all driver outputs provide a minimum of 6.5VDC output with maximum control input to the card.

L. Verify that all outputs provide zero output (no pulses observed on the scope) with the control signals returned to zero.

M. Seal all potentiometers with Glyptol or other suitable means.

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