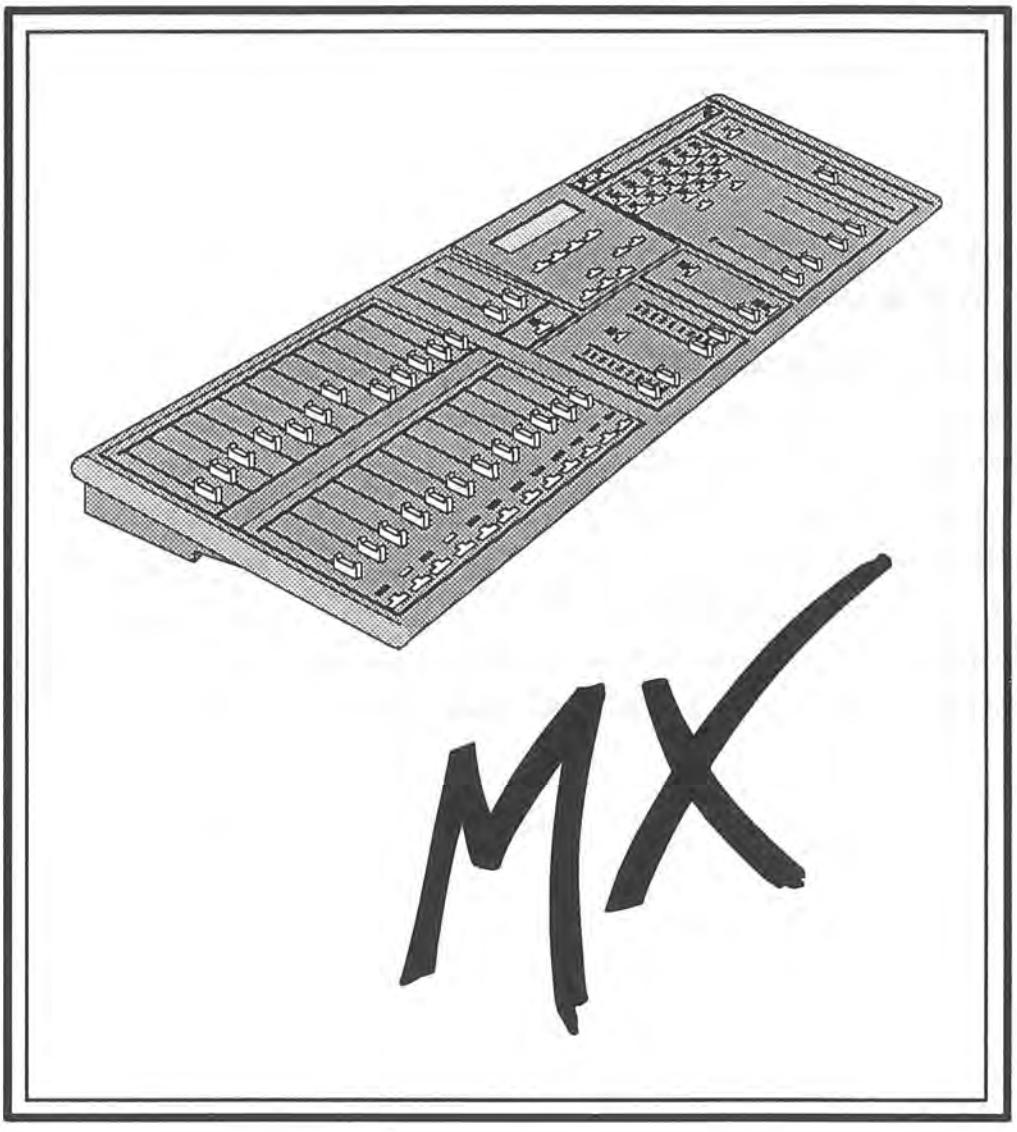
CIRCUIT INFORMATION



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Introduction

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Introduction

1 PURPOSE

The purpose of this document is to describe the hardware of the MX console range in detail.

2 SCOPE

This document, together with the associated circuit diagrams, should impart enough information about the hardware for service and test. A part of this document is the test specification for the MX range of products.

The reader is assumed to be familiar with lighting concepts and the terms such as DMX512 etc. Information may be found in the references.

3 OVERVIEW

In order to make the circuit design manageable, the hardware can be split down into functional blocks.

Section B describes these functional blocks and describes how these blocks are related. The inputs and outputs of each block are described, with references to related documents for further detail. Any relevant assumptions and calculations are contained here.

Section C describes the signals that pass between the various functional blocks and what controls each, its reset [power-up] state and any special information relating to the signal. This is primarily for software reference.

Section D details the memory map.

Section E is the test specification for the MX product range. This covers what is required of the in-circuit tests and functional tests which are strongly related to the Built-In-Self-Test - BIST - functions of the software.

4 REFERENCES

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[22] Circuit diagram 6B 40045 Control PCB

[23] Circuit diagram 6B 40046 Fader PCB

[24] Logic source files 7X 33390 Control PCB: IC's 28, 31

Functional Block Description

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Figure 1 D54 / AMX Timing Signals

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Functional Block Description

1 GENERAL

The general design principles are discussed in the System Architecture document (ref. [2]). This description splits the circuitry up into the processor PCB which contains all of the processing electronics, power supply, interfaces and connectors, and the fader PCB, of which there may be up to 4 in a system.

2 PROCESSOR PCB

The processor PCB is split into functional blocks according to the schematic drawings. These are each given individual sections, and at the end of each section and there is a description of the (BIST) test facilities offered by each functional block.

2.1 Processor

2.1.1 General

The processor is an 80C196KC. This is the latest version of the 80C196, an upgrade from the 80C196KB. The processor runs with a 16MHz maximum crystal and a very fast external bus. This leads to the requirement for use of AC series high speed CMOS in most areas of the processor logic (refs. [13], [14] & [15]).

The processor includes all the MCS–96 I/O, but with the extra features of 2 extra PWM outputs and the Peripheral Transaction Server which allows faster interrupt response. The two extra PWM outputs are used to drive the LCD contrast and backlight intensity.

2.1.2 I/O Facilities

In order to reduce costs, all on–chip I/O facilities are used in this implementation. The input and output ports are used to control specific I/O devices. The HSO is used to generate timing synchronisation signals for the dimmer analogue multiplex signals and a test signal for the audio processing circuit. The HSI is used for time–stamped inputs and other interrupts. The A/D converter is used for reading the fader values and for testing parts of the circuit.

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2.1.3 Memory

2.1.3.1 General

The 80C196KC bus is extremely fast, therefore in order to run without wait states, the memory has to have a very fast access time. The INST pin is used to expand the total address space available to the application code. Two 64K x 8 EPROMS (27C512) are used and these are configured to be word wide to get the best performance from the processor. Timings are dependent on the memory decode delays, and these are set by the decode devices (see below). To run without wait states, the EPROMS need to have 100ns max. access.

For the 12/24 way versions, 1 wait state is inserted, as these cannot stand the cost penalty of 100ns devices. In order to meet the timing requirements with 100ns parts, a pair of tri–state buffers, IC's 30 & 33, were added to reduce the output enable delay time.

The analysis provided in the System Architecture Document (Ref. [2]) shows that 32k x 8 SRAM is required as a minimum. The design allows for a pair of these devices to be used so that expansion is possible without laying a new PCB. Because of the high speed bus, it was not possible to economically design 0 wait state RAM into the system. Therefore 16 bit RAM with 1 wait state was implemented, with 2 devices fitted from the outset. Critical elements of the code use internal registers to speed operation. When the protected RAM area (controlled by the GAL programming) is write–protected, it is READ with 0 wait states.

All I/O, including the memory card, is run in 8 bit mode. The processor's buswidth is dynamically changed by the memory decode GAL's using the buswidth pin.

2.1.3.2 Memory Map Decoding

In order to provide maximum flexibility and cost effectiveness, a pair of GAL20V8–15 devices (IC28, 31) are used to decode the memory map.

The devices generate the necessary wait states for the READY pin. See the section on memory map for exact memory mapping. The processor provides two output port pins to allow it to page the code part of ROM, and control the number of wait states. On the 48 way version 100ns ROM's are fitted and the processor switches these into 0 wait state by setting the ROM WAIT pin low. It defaults to high – 1 wait state – at power up.

An extra 3 to 8 line decoder, IC 32, is used to generate the peripheral enables to a high resolution so as not to waste address space. All peripherals run with 3 wait states. 1 wait state adds 1 CLKOUT cycle to a given memory access.

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2.1.4 Memory Card Interface

The memory card interface is derived from a Mitsubishi application note MDS–MEMCARD–07–9–88–250. The circuit allows the card to be inserted while the system is powered up, and also allows the power to be switched on and off while the card is inserted. All lines to the card are buffered by tri–state devices, these being controlled by the card detection signal (/CD) and /RESET gated together. This ensures that:

a) The signals are not enabled until the card is in place (because of the /CD contact and switch–on delay).

b) During **MX** power up/down sequences the lines are tri–state.

The /CD signal is schmitt triggered with an RC input network to ensure reliable control.

The power to the card is also controlled by a transistor VT 13, enabled by the above signal.

Data is controlled by a bidirectional tri–state buffer, IC38, a 74HC245. Its direction is controlled by the /RD signal and it is enabled by the above signal gated with a decoded /CE_CARD signal.

The full address range of the card is catered for by a page register IC41, a 74AC573 latch. This has a tri–state output controlled in the same way as the above data and address buffers. Before reading or writing to the card, this page register is loaded with a high order 8 bit address by a uniquely decoded memory address. This solution provides 255 2kbyte windows onto the card giving a 0.5Mbyte possible max. addressing range allowing the use of larger cards in the future. **MX** uses 64Kbyte cards initially.

The status signals from the card are all fed to the DUART's input port for reading by the processor. Mitsubishi cards give 2 pieces of information that other cards do not generally give. These are:

The WP output. This tells the system, when high, that the card's write–protect switch is on and the card cannot be written to. The card protects itself, even if writes are attempted.

The B0, B1, B2 outputs. These tell the system what type of card is connected. The codes are as follows:

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	B0	B1	B2
RAM	0	0	0
OTP ROM	0	1	0
Mask ROM	1	0	0

In the MX system, these are connected to IP4, IP5, IP6 respectively.

2.1.5 Test Facilities

The memory card interface incorporates the facility to allow the card battery voltage to be read. The processor reads this via a multiplexer that is powered from V_RAM (See 2.2.5). The card voltage should be read in the A/D's 10 bit mode and is O.K. if above 2.60V. (Mitsubishi figure).

2.2 PSU

2.2.1 5V Switching Circuit

The heart of the power supply is the switching regulator, the STM L4963 (IC10). This chip fully implements a buck converter and includes all the necessary power handling circuits. It is ideal for MX because it incorporates power fail and reset circuitry also, with a minimum of components.

2.2.1.1 Input

The circuit runs off a 15V nominal supply, this may be 23V off load and its worst case load must be >= 15V. The input is filtered with a 2200µF cap. and contains a 1.35A polyswitch and 1.5kW/5W transzorb with a maximum clamping voltage of approx 43V. This provides over/reverse voltage protection. The polyswitch will hold 1.0A continuously at max. operating temperature (35°C) + internal temperature rise of 15C. A twin hole bead, L16, is wound with two windings in phase opposition to attenuate mains–borne asymmetric RFI.

2.2.1.2 Power Fail

The power fail element of the L4963 (pin 7) has a threshold of 3.6V falling and 4.4V rising. A precision external voltage divider is placed around pin 7 of the chip to raise the thresholds to 10V and 12–12.5V respectively. This is a low impedance divider to swamp the internal divider to reduce tolerance errors. The low going threshold is set to allow 1V before the L4963 falls out of regulation. In practice

this was measured as 8V, but the spec. gives a worst case 9V. This 1V fall requires a 2000µF capacitor minimum to provide the System Architecture's requirement of a 2ms warning period, assuming a constant current load. The 2200µF capacitor provides enough reserve. The 10V level provides for an allowable supply droop of approx. 30%, more than is required by the design spec. because it was thought at design review that the board should work with a 240V transformer on a 220V supply and should therefore work to 198V.

Power fail is also connected to the enable of the decoder driving the source transistors for the LED's. This disables the LED's at the instant of power fail and therefore extends the available warning period to approx. 4ms.

2.2.2 +9 / –9V Regulator

MX requires both positive and negative rails for D54, RS232 and analogue signal buffers. The ideal voltage is around 8.5V to give RS232 signals of sufficient amplitude, without making the D54 driver dissipate too much power. At least 8.5V is needed on the positive rail to allow for voltage drops in the D54 driver which must be able to output 6V (nominal +20%).

The solution was to wind a pair of secondaries on the main inductor, creating a pair of flyback converters to generate a nominal +/–14V. This is then regulated down to + and –9V by a pair of 7809 regulators. The stacking configuration of regulators is used as it was possible to provide a pair of isolated secondaries without extra expense over a split secondary, and this lowers the component count.

14V is required to maintain regulation with the worst case input of 10V and lowest load current. The current needed is approx 40mA on the negative rail and 90mA on the positive rail (the asymmetry is caused by D54 signals). The devices incorporate thermal shut-down protection and over current foldback protection. 78 series regulators are used as power dissipation could be a problem in the worst case, particularly on the positive rail.

2.2.3 Battery Back–up

2.2.3.1 Back-Up Power Source

The CMOS RAM in **MX** is supported on a 3.6V Ni–Cad cell.

2.2.3.2 Back-Up Circuit

The back–up battery is switched into the V_RAM supply by a simple silicon diode D18, dropping approx. 0.6V. V_RAM must be at least 3V so that the

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memory card, if left connected, is not discharged by the A/D multiplexing circuit. The battery is charged at a current of approx. 3mA. This current is above the normal trickle charge as the operation of the product is somewhere between standby and cycle. V_RAM is connected to the 5V rail by VT1, the circuit ensuring that V_RAM is always at 5V during normal use, giving maximum noise immunity.

A prototype PCB yielded a 1.6µA back-up current at 25C.

2.2.4 Memory Protection

As part of the Architecture, **MX** incorporates comprehensive memory corruption protection. The RAM chip select (active low) is driven from a 74HC00, IC21, which is powered from V_RAM and only consumes approx. 1µA on standby and will operate down to 2V. /RESET is gated by the HC00 so as to guarantee that upon reset the memory chip select becomes inactive high. The L4963 ensures that RESET falls before the 5V rail goes out of tolerance.

2.2.5 Test Facilities

MX is equipped with a test connector to allow voltage measurements to be taken at one place. All power rails and internally generated references are available on this connector, as are the two processor test inputs. The test inputs are deliberately not buffered (or debounced) so as to retain the minimum amount of hardware between the processor and outside world for the PCB functional tests. The power supply may be turned on and off by use of the /INH signal. When held low, this turns off the L4963 and hence the other rails, allowing remote supply cycling and making a memory retention test easier to perform.

The power supply circuit also permits the processor to sample the relevant signals to perform its internal diagnostic tests. There is a particular problem with this approach where the battery voltages have to be sampled. The multiplexer has to be powered from the V_RAM supply so that V_RAM does not attempt to power the rest of the board via the multiplexer protection diodes. The worst case standby current is 5µA for the 4051 and this is an acceptable drain. One gate of IC21 is used to disable the multiplexer in reset.

Unfortunately, the processor A/D has a worst case DC leakage of 3µA and this could result in a 0.3V (10%) drop at the A/D. Hence the battery back-up voltage is fed back to the multiplexer via 470R as well as a 100k resistor. This allows the processor to check its input leakage current by comparing the two voltages. The voltage read on CAL_VOLTS can be assumed to be accurate regardless of leakage (within the power supply reference tolerance of +/–2%). Having read the

value of BATT_VOLTS and taken the difference, CARD_VOLTS can be measured, and since the input resistors are equal in each case, the difference directly added to arrive at the absolute card voltage.

This method saves a buffer IC and associated components, and since these voltages are read infrequently, has no performance implication. Since the card voltage and back-up voltage are of similar magnitude, the method is accurate. The difference should be measured each time the card voltage is read, as temperature fluctuations will be significant as far as input leakage is concerned.

2.3 Comms

2.3.1 DUART

The Duart used in **MX** is the SCN2692. This is functionally similar to the familiar 2681 chip, but is fabricated in CMOS. It provides the majority of the I/O associated with the various comms links, analogue and digital. The two asynchronous link requirements are:

1 MIDI – full duplex, fixed baud rate: 31250, 1% tolerance

2 RS232 – full duplex, variable baud rate up to 19200, 1% tolerance

MIDI was allocated to channel A, RS232 to B. Unfortunately the two baud rate range(s) are not achievable with one clock source because of incompatible division factors. The solution is to supply 4MHz divided from the CLKOUT of the processor (8MHz) to the internal timer/counter of the chip. The timer/counter can be set to give exactly 31250 baud. The RS232 links are supplied by the DUART's own crystal oscillator at the obscure frequency of 3.6864MHz. The Duart provides its own fixed dividers from this frequency to generate all the required standard baud rates accurately up to 38400 baud.

2.3.2 Reset

In common with the 8279, the 2692 requires a positive RESET signal. This could have been derived from the /RESET signal, but the signal would be very short (16 state times = 2µs) and the 8279 does not quote a minimum acceptable time. Therefore a processor port pin generates the signal PERIPHERAL_RESET. The port pin automatically goes high on reset, software must pull it low to operate the peripherals.

2.3.3 D/A

The D54 and AMX92 dimmer drives require a D/A converter. The DAC08 was chosen. It does not have a bus interface, so is connected to the 2692 output port. The details of this connection are discussed in the section on pin allocations.

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The DAC08 provides a Vlc pin to set the operating threshold of the logic inputs to make them compatible with many different logic families. In this implementation, the pin is used as an enable, /D_A_ENABLE. The device guarantees that the logic threshold levels will be 1.4V typically and 1V worst case above Vlc. Hence by connecting /D_A_ENABLE to HSO.0, the processor has effective control of the D/A, with /D_A_ENABLE high the D/A output is forced to 0.

The DAC08 is a current based converter and therefore requires a reference current. In order to provide the user with the facility of being able to trim the analogue output voltage from the LCD (to compensate for line drops and dimmer matching) and implementing the philosophy of removing all preset pots. from the system, the reference current is processor derived. The Design Specification requires a +/– 20% variation. This is achieved by integrating one of the three pulse–width–modulation (PWM) outputs (PWM_0) over a sufficient time so as to produce a DC voltage with less than 0.5 LSB ripple. The converter provides a multiplying function between this reference and the digital input byte, therefore controlling the effective maximum output current with the PWM value.

The PWM frequency is set to the highest possible with this aim in mind (31250Hz @ 16MHz), and is integrated using a 3k3 resistor and 10µF cap. The time constant of the reference network is therefore 17ms since the voltage is converted to current by another 3k3 resistor (to keep analysis simple) and the DAC08 reference input is a virtual earth. Using the data sheet values for the Voh of the PWM output, it will provide approx. 4.8V at the reference current. In order to provide the +20% headroom, the standard PWM output will be 200 decimal. This is divided by two by the reference smoothing network to give 1.88V, giving a standard reference current of 0.57mA, peak about 0.73mA. The recommended range is 0.2 to 2mA, and keeping on the lower edge keeps power supply current low and reference smoothing capacitor small. The positive input of the reference amplifier is connected to analogue 0V; no resistor is used to compensate for the worst case 3µA bias current, as this is only approx. 1 LSB.

The output current is converted to output voltage by the output amplifier.

2.3.4 Analogue Synchronisation Signals

Different synchronisation pulses are needed to generate D54 and AMX192 dimmer control signals. The electrical requirements are different, but the timing of the relevant control signals is very similar. Fig. 1 shows D54 and AMX sample waveforms and the control lines that generate them. The HSO's were seen to be particularly suited to generating these control signals as they must be precisely timed pulses.

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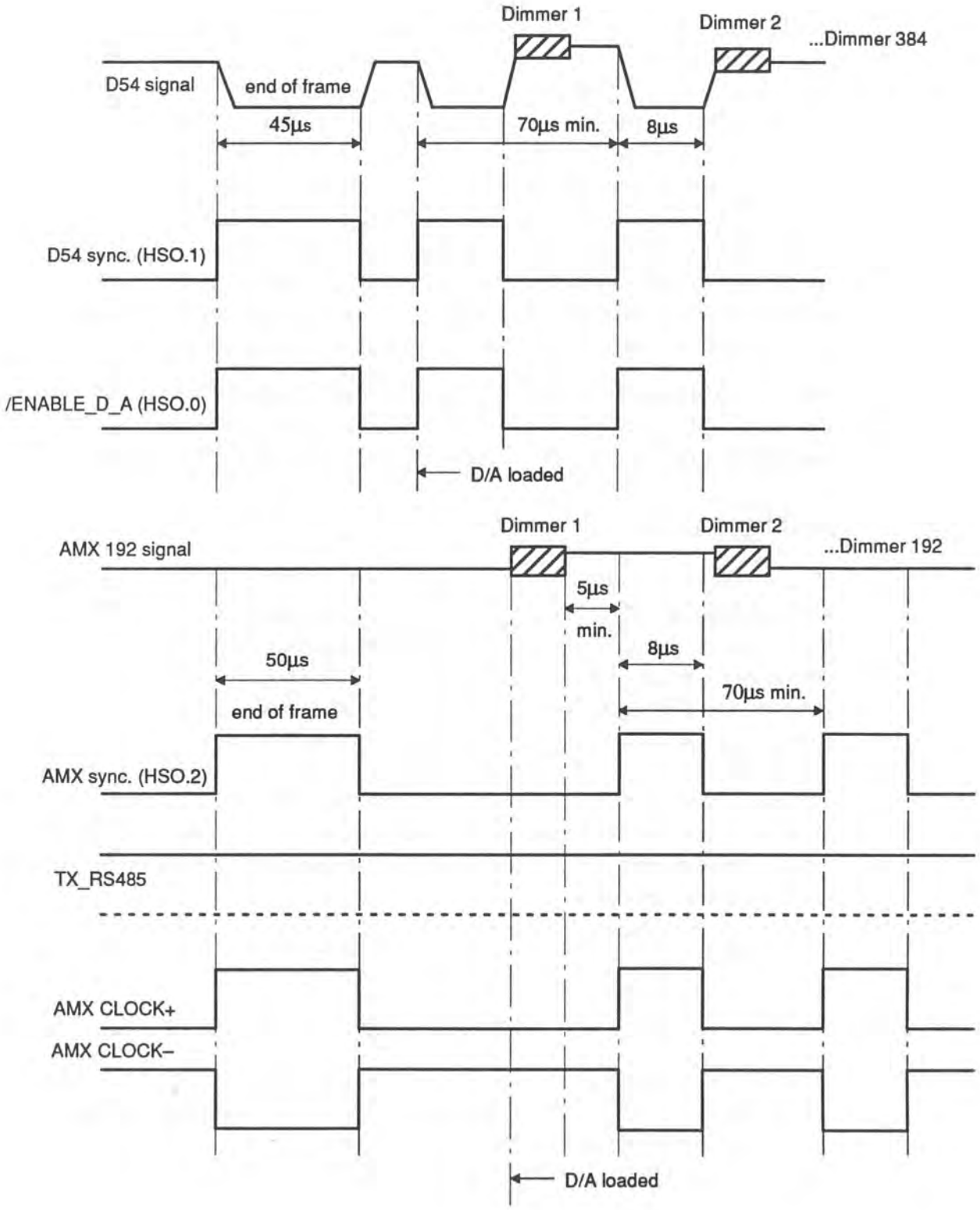

Figure 1 – D54 / AMX Timing Signals

HSO.0 and HSO.1 were chosen to drive /D_A_ENABLE and D54_SYNC respectively, as they can be driven together in one HSO instruction. This allows the processor to set up the D/A and generate the D54_SYNC at the same time, without having to return to service the end of the sync. signal. It also gives a fast transition between the sync. and the analogue level. The sync. is generated in the form of a current defined by Voh of the HSO output – 0.6 (diode drop) and the reference resistor(s). A pair of 3k3 resistors were used, resulting (when the D/A is disabled) in a output sync. pulse of approx. –5.5V, allowing plenty of headroom for any D54 receiver. The arrangement algebraically adds the D/A output current (negative) and the reference current (positive) into a virtual earth – the hardware does not have to combine sync. and D/A output with analogue gates.

HSO.2 is used to generate AMX_SYNC and is gated with the TX output of the processor. This signal drives the RS485 transceiver, IC8. The two signals are NANDED, so to use TX, HSO.2 must be high, to use HSO.2, TX must be idle.

2.3.5 Analogue Drive

This section of the COMMS circuit consists of 1/4 of a TL084 op–amp coupled with an LM6321 buffer amp. The TL084 provides an almost ideal op–amp for the low current output of the D/A, and is arranged as a virtual earth current to voltage converter. Enclosed in its feedback loop is the LM6321 buffer (IC7). This device provides +/– 300mA drive and is stable into very heavy capacitive loads. It is purpose designed for driving long lines. It incorporates current limiting and thermal shut-down protection. Voltage protection is provided by a bidirectional 12V transzorb, D17, with its capacitance providing half of the LC RFI rejection network. The D54 output requires a source impedance of 4R7, the AMX output, 100R. The same amplifier is used for both as the protocols are supported on a mutually exclusive basis.

The standard output current has to be converted to +5V by the resistor in the feedback loop of the amplifier, hence this resistor is:

$$5/.057 = 8.77k$$

An intelligent feedback system is used to set the PWM value, and this compensates for differences in processor Voh values and de–sensitises the requirement for the accuracy of this resistor. Even so, 2% components are used in the whole subsystem so as to limit the possible tolerance build up. An 8k2 resistor is used.

2.3.6 RS 485 (DMX/SMX)

The RS485 output provides the several mutually exclusive functions on MX:

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1. To drive the SMX protocol. This is achieved with the 80C196 UART.

2. To drive the DMX512 protocol. This is achieved with the 80C196 UART.

3. To drive the AMX192 sync. pulses. The HSO.2 output of the processor is used for this function. 100R resistors are used in series with the outputs as the AMX spec. requires.

The IC used is a standard 75176. The receive function is permanently enabled as the receive section of the processor UART may be disabled internally. Protection is provided against transients with transzorbs across the driven lines to ground. These, together with inductors, provide RFI protection.

2.3.7 RS 232/RS 485

The RS232 port is implemented with a 75155 single channel transceiver. This is powered from the +/– 9V rails which produces a signal range of approx. +/– 7V. This is sufficient to maintain the +/– 3V swings required by the RS232 specification. Protection against interference and voltage transients is again provided by transzorbs and inductors.

It was decided (in the Design Specification) that modem control lines would not be implemented, as this would only serve to complicate the software, increase the cost of the hardware and give the user no real added benefit. However, as **MX** acts as a DCE, the DCE's required output modem control lines (pins 5,6 and 8) are pulled high (active). Sometimes receiving equipment locks out if these lines are not valid, this prevents that situation occurring.

This port also has an RS 485 transceiver (75176) to enable direct use of SMX. Its transmit and receive functions are separately enabled by /ENABLE_RS485_TX and /ENABLE_RS485_RX, allowing comprehensive loopback tests. The gating arrangement around IC 35, 21, 23 toggles the RXDB line between the RS232 transceiver and RS485 transceiver. The application software can decide on the receive source and can turn the line around during SMX comms. The RS485 transceiver and associated components are not fitted for /B (standard) build.

2.3.8 MIDI

The MIDI interface is implemented using variants of the circuits detailed in the MIDI specification. The optocoupler chosen is the GE H11L1, as it provides the required sensitivity (1.6mA), is specified to work up to 1 Mbaud, and incorporates a schmitt trigger output. Using this, rather than a darlington output device, results in better rise/fall time control, and turn on/off time ratio. It is this factor that governs the durability of the interface because the signal becomes

more asymmetric, the more MIDI devices it passes through. The absolute skew is irrelevant, but the asymmetry is not. The H11L1 specification states:

Ton = 0.65µs, Toff = 1.2µs

This would only result in 2% asymmetry.

The actual figures achieved depend on the matching of the drive current to the LED. The input resistor has been increased above the MIDI spec. to 820R, to reduce saturation, giving a good performance at 2.5mA. In the actual application (5mA worst case), there is still approx. 100% overdrive, this being maintained to allow for LED degradation over time and component tolerance. The figures achieved were:

Ton = 900ns, Toff = 2.5µs, giving a 5% asymmetry

The through and output signals are driven by a 74AC14, IC3, capable of supplying 24mA, and a lower level of voltage protection is supplied by BAS16 clamp diodes. RFI protection is provided by the series inductors. The MIDI interface was seen to pose less of an interference and transient hazard as it only involves connection of short cables in temporary installations.

2.3.9 Test Facilities

In common with the other elements of the circuit, the COMMS circuits incorporate extensive test facilities.

2.3.9.1 DUART

The DUART has the internal capability to allow most of its registers to be read back by the processor. This should give adequate indication of DUART operation.

2.3.9.2 D/A, Analogue Drive and Synch. Signals

There is no direct test on the D/A converter itself, as being current based, it is a little difficult to test! The output of the analogue driver is fed back to an analogue multiplexer for sampling by the processor A/D. This allows a functional test of the D/A and driver block as a single entity. The input is protected by a 4k7 resistor and diode clamps. The 10 bit resolution of the A/D could allow monotonicity tests to be performed.

The D54 synchronisation signals can be tested by splitting the control of the HSO.0 and HSO.1 signals. By enabling the D/A (/D_A_ENABLE = low) and

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setting the sync. signal (D54_SYNC) high, it is possible to perform an additive function between the D/A and the sync. current, using the read–back A/D input to check the result.

The D/A reference signal, D_A_REF, is also fed back to an analogue multiplexer, this allows the processor to check that both the PWM and integrator are working, and the absolute value of the reference for setup purposes. The accuracy will be limited by the power supply reference tolerance of +/–2%.

2.3.9.3 RS 485 (DMX/SMX)

As indicated in the RS485 section, both RX and TX are permanently enabled, this allows the processor to read the actual RS485 data that it is transmitting without use of loopback connectors.

2.3.9.4 RS 232/RS 485

The RS232 drivers require loop back connectors to be used to check their operation. The DUART has to transmit data out of the B port and check it on reception. This port also has an RS485 transceiver and this has 2 control lines /ENABLE_RS485_TX and /ENABLE_RS485_RX. To perform a test on this port, both the functions need to be enabled. The act of enabling the RS 485 receiver disables the RS 232 receiver. The /ENABLE_RS485_TX signal is arranged so that the line is tri–state during and after reset.

2.3.9.5 MIDI

The MIDI interface drivers are tested in the same way as the RS232 drivers, loopbacks being used so that the processor can transmit and receive its own data.

2.4 Audio

The Audio input to MX provides comprehensive automatic level control to assist the user. This circuit is arranged so that it meets the Design Specification's requirements for a 60dB dynamic range; this is achieved using a Philips NE571 compandor in ALC configuration.

2.4.1 Input

The front end of the circuit consists of a differential amplifier based on a TL084 with a gain of approximately 0.5 and 6dB/octave roll–off above 20kHz. The input is AC coupled in both signal and ground lines and has RFI suppression using

appropriate LC networks. This gives the input immunity to noise, DC and 50Hz common–mode signals. The left and right channels are algebraically added in this configuration.

The ALC circuit generates a standard 0dBm signal (0.775 RMS) and the minimum accepted signal is –43dB from this level (43dB is approx. the max. gain available). This represents a signal of 5.5mV RMS. The maximum level seen by the compandor will be approx. 11V peak–peak (3.8V RMS), determined by the limit of the TL084 output. The gain of the input circuit, has to be set so as to allow approx. 10mV to 10V RMS to be accepted.

The gain of the input circuit is set to 0.5 so that the compandor just about sees sufficient level at 10mV RMS input and works linearly up to the maximum possible level of +14dBm.

2.4.2 Filter

The filter circuit follows the input circuit and is placed before the ALC circuit so that mid and high frequency signals do not affect the gain control. This is a simple, unity gain, maximally flat, 12dB/octave low–pass filter, rolling off above 200Hz.

2.4.3 ALC Circuit

The ALC circuit is built around an NE571 compandor. The design is based on application notes AN174 and AN176 for an ALC, with suitable adjustments. The ALC is constructed around one half of the chip. The adjustments that were made were:

1. Rdc set to 15k to set the output to +3.6V so that the DC operating level is satisfactory for an 9V supply.

2. Crect set to 10µF to give a 100ms time constant. The attack time will be faster than the decay time according to fig. 9 of AN174 (as required by the Design Specification). With this configuration 100ms was found to provide a good subjective response.

The other half of the chip provides an ideal output rectifier from the ALC, as the precision rectifier element can be accessed independently of the other elements. The signal is AC coupled into the rectifier, and in order to provide the Design Specification's required response, a diode is included in the output. This subtracts a fixed voltage from the (smoothing) capacitor signal, but since this signal is approximately constant (ALC action), it can be compensated for with extra output gain – this is not Hi– Fi! The diode does have the added advantage of giving a small amount of noise immunity. The rise time of the signal on the 1µF

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smoothing capacitor is 10mS, determined by the chip's output impedance, its fall time is set to 50ms by a 47K resistor.

2.4.4 Output

The maximum output of the ALC circuit is in the region of (2V – 1 diode drop), ie approx 1.5V. In order to provide a 5V signal for a schmitt trigger, the signal is amplified with a gain of approx. 3.5 using 1/4 of the TL084. The signal is dioded onto the Audio/MIDI 10k pot. RV8, together with a MIDI_ENABLE signal. This configuration is used to:

1. Allow the use of only 1 type of pot. in the whole product.
2. Allow MIDI timing signals to be controlled (in software).
3. Allow the processor to check the position of the pot during Audio Test procedures.

The configuration is arranged so that MIDI takes precedence. It was not thought worthwhile providing simultaneous Audio and MIDI control.

A schmitt trigger is used to provide interrupt edges to the processor HSI.2 pin. This allows software separation of audio level and effects stepping.

2.4.5 Test Facilities

One of the processor's HSO outputs is divided and AC coupled into the non–inverting side of the differential amp input stage. This provides a test input to the audio processing subsystem when the HSO generates suitable frequency squarewaves. The frequencies are programmed to test the roll–off of the filter circuit and check for adequate gain. **Clearly any audio source must be disconnected during this test.** The divide ratio is set to 400:1 as the differential amp. will behave as a unity gain buffer in this configuration. The resulting signal will be approx 6mV RMS at the ALC (in the pass band of the filter).

2.5 LED Drive/Keyboard Control

The keys and leds on the control PCB are controlled by an 82C79 keyboard/display driver IC20. This is a clocked synchronous logic block that continuously scans the keyboard and refreshes the LEDS. It is used in default display mode (16 character, 8 bit display) and in encoded mode, with the keyboard in sensor mode.

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The clock rate is set to 80KHz by an internal software controlled prescaler, which divides down the 2MHz basic clock provided by division of the processor CLKOUT.

2.5.1 LEDS

The 82C79 addresses a 16 x 8 array arranged as 16 sources decoded from four scan lines, and eight sinks. In this implementation, the first 8 sources are actually on the fader PCB's, the last 8 are on the control PCB (VT2–9). All sinks are provided by IC17. On the control PCB, IC14 decodes the last eight states of scan lines SL0–3, IC13 decodes the first eight for the fader PCB's. Inter–character blanking is provided by the chip (/BD goes low), and this disables all drives (IC13, 14), so removing the possibility of crosstalk between columns.

Because the multiplex drive is nominally 16:1, which is in reality approx. 20:1 when the inter–character blanking is taken into account, the LED's have to be driven with a reasonably high current. This is set by the 4R7 resistors attached to IC17, and IC17's saturation voltage and the saturation voltage of VT2–9. Approx. 100mA was chosen giving an average of approx. 5mA. The LED's chosen are moderately high efficiency and are intensity matched for the 3 colours.

2.5.2 Keyboard

The scan lines SL0–3 are also decoded by IC15 to provide the drives for the keyboard array. Each row is selected individually as the scan counter increments, and depending on the key pressed, a code is read into the sensor memory of the chip. Diodes are provided on each switch to prevent interactions if multiple keys are pressed. The scan process is continuous and results in eight bytes (of which only 5 are used) in the 82C79 containing the image of the keys pressed. An active key appears as a 0 bit. This method is chosen, as opposed to the debounced FIFO mode, so that the software can detect how long a key is held on, allowing it to perform the auto–repeat functionality required in the spec. Software also debounces the keys by reading the sensor image array at 5mS intervals.

3 FADER PCB

The fader PCB is designed so that it can be used in any of the four required positions in the system with just one switch change. It is also designed so that all four PCB's can be daisy–chained on a single piece of ribbon cable from the processor PCB. This cable carries a six bit address allowing 24 faders and 12 switches to be addressed, the LED matrix signals, and power supplies. A separate supply is provided for the LED matrix to reduce noise problems.

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The ANL_GND connections are interleaved with the analogue lines out (ANL_[0:3]) to minimise cross-talk. The remaining signals are then graded in order of least to most hostile away from the analogue lines in the ribbon cable.

3.1 Address Decoding

The PCB address is set by the 2 pole/4 way switch. This switch uses 1 pole to connect the relevant analogue multiplex signal to the analogue bus and generates 3 control bits with the other pole. This 3 bit address is fed into a pair of 4051's used as selectors to connect 2 of the 8 column drive signals CA_0 to CA_7 to the drive transistors for the LED's.

There is no per–PCB addressing of the analogue sections of the fader PCB's, as there is a dedicated analogue line for each PCB.

3.2 Analogue Multiplexing

The analogue multiplexers are supplied with a parallel 6 bit address (via R7–12 to protect against ESD damage). The lower 3 bits of this address are supplied in parallel to each of the 5 4051 analogue multiplexers. A further 4051 multiplexer takes the 3 upper address bits and multiplexes the 5 multiplexed signals onto one CMOS buffer, a CA5160. This is used because it can output 0V without a negative supply and can output 5V on the +9V analogue supply. A buffer was necessary because of the intrinsic high impedance of the signal, its increased impedance having gone through 2 multiplexers and the inevitable noise down the ribbon cable. N.B. The LED switching noise is not a problem because of the architectural precautions taken (Ref. [2]).

3.3 Flash Switches

The flash switches are multiplexed in the same way as the faders and are read as faders. Because the 4 analogue lines are fed direct to the processor port 0, the 80C196 can read the switches in a digital manner. This is convenient because the 4 switches from the 4 possible fader PCB's are read simultaneously by reading port 0. Debounce is done in software.

3.4 LED Drive

The addressing effectively selects 2 sequential columns of the 16 total addressed by the 82C79 for each fader PCB using ICs 2,6. The source drivers are on this PCB as it was easier to select the address than to select the high current drives. The sink drivers are the ones on the control PCB. The LEDS are arranged in 2 rows of 6.

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The peak pulse current, being set by the row sink drives, is the same as that on the control PCB. It is set at approx 100mA, as the mark/space ratio will be approx 20:1 as generated by the 8279, giving an average of approx 5mA. The LED's chosen are moderately high efficiency and are intensity matched for the 3 colours.

3.5 Test Facilities

There is no specific input on the processor to tell the software which model of board it is controlling. This is done by the test facilities of the fader PCB. The software will check the 3 test locations of each PCB at power–up. It should find a sequence of 5V (–10%), 2.5V (+/–10%) and 0V (+10%). The tolerances allow for resistor tolerances and A/D offsets. This unambiguously indicates the presence of a fader PCB – hence product identity – and the operation of the addressing and multiplexers.

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Signal Descriptions

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Signal Descriptions

1 PROGRAMMABLE I/O PINS

The Hardware Architecture of **MX** results in a large number of programmable I/O pins, these being found on the 80C196 and the DUART, the 2692. The philosophy has been to use these wherever possible to eliminate I/O port chips and associated memory decoding. The sections below indicate the uses of these pins.

1.1 Processor

1.1.1 I/O Drive

The processor has a large number of I/O pins some of which are configurable to perform special I/O functions, some of which are general purpose I/O, some of which are solely inputs or solely outputs. The Intel manuals are do not group all this information in one place so it is difficult to determine which pin to use in some cases, especially as there are three variations of electrical properties:

Quasi–bidirectional – I/O

will pull low to:	0.45V at 2.8mA 1.5V at 7mA
will pull high to:	Vcc–0.7 at 30µA Vcc–1.5 at 60µA

as inputs – leakage = +/– 10µA

Input only (port 0)

leakage = +/– 3µA

Output only

will pull low to:	0.45V at 2.8mA 1.5V at 7mA
will pull high to:	Vcc–0.7 at 3.2mA Vcc–1.5 at 7mA

1.1.2 Allocation

The choice of I/O pins was made by first defining the use of the special pins, using them in the most effective way for **MX** software and the processor's I/O

capabilities, then defining the input only and output only pins for uses that could only ever require inputs or outputs, then defining the rest with general purpose I/O pins.

In **MX** all the I/O devices of the processor are used to their full extent thereby realising the power of the architecture. This fixes the use of:

UART – RX, TX pins

HSO – 4 HSO pins

HSI – 4 HSI pins

A/D – All of port 0

PWM – P2.5, 1.3, 1.4

NMI

EXTINT – P2.2

T2CAP – P2.7

TEST INPUTS – 2 input only pins, must be direct to the processor

Two inputs can be either HSI and HSO pins. In this case 1 of each mode is selected. HSI inputs are particularly useful because they allow a events to be time stamped, so reducing interrupt latency problems.

HSO.0 and HSO.1 were chosen for D54 sync. generation as they can be programmed to act together for easy software drive under normal conditions, but can be driven separately for test purposes. The section on COMMS details their use.

The allocation is detailed below, with the reset state shown for each pin. If the pin is driven by external hardware, the state is shown in brackets:

PORT PIN	FUNCTION NAME	RESET STATE	COMMENT
P0.0	FADER_PCB_1	X	Multiplexed faders and buttons
P0.1	FADER_PCB_2	X	
P0.2	FADER_PCB_3	X	
P0.3	FADER_PCB_4	X	
P0.4	MPXR_SIGNAL	X	Other i/p's from processor PCB
P0.5	Vcc/2	X	Reference voltage tocheck A/D
P0.6	AUDIO_LEVEL	X	Averaged audio signal
P0.7	GM	X	Grand master level
P1.0	/ENABLE_MIDI	1	Low drives Audio/MIDI pot. to +5V
P1.1	/ENABLE_RS485_TX	1	Low enables RS485 TX
P1.2	/ENABLE_RS485_RX	1	Low enables RS485 RX (disables RS 232)
P1.3	/LCD_CONT	1	PWM_1 – LCD contrast
P1.4	/LCD_LIGHT	1	PWM_2 – LCD backlight level
P1.5	PERIPHERAL_RESET	1	High to RESET 82C79, 2692
P1.6	PAGE SELECT	1	selects top 32K ROM code space
P1.7	ROM_WAIT	1	high = give 1 wait state, low = 0 wait state
P2.0	TX_RS485	0	RS485 transmit
P2.1	RX_RS485	X(0)	RS485 receive
P2.2	2692_INT	X(0)	DUART int signal (+ve edge)
P2.3	M1	X(1)	Test mode input 0
P2.4	M2	X(1)	Test mode input 1
P2.5	D_A_SET	0	PWM_0 – D/A reference voltage
P2.6	/ENABLE_RAM	1	Low enables RAM protected area
P2.7	POWER_FAIL	1	T2CAP – processor has less than 2ms to live
HSO.0	/ENABLE_D_A	0	Low enables D/A converter
HSO.1	D54_SYNC	0	High adds –5V to D/A output
HSO.2	AMX_SYNC	0	High drives RS485 true (provided TX=high)
HSO.3	TEST_AUDIO	0	Squarewave adds signal to audio input
HSO.5	TEST_LED	0	High drives test LED on
HSI.0	LED_SYNC	X(1)	/BD of 8279, low when blanking
HSI.1	8279_INT	X(0)	+ edge on 8279 key entry
HSI.2	/AUDIO_TRIG	X(1)	– edge on music beat
NMI	MEM_CORRUPT	X(0)	+ edge = attempted illegal memory write

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1.2 DUART

1.2.1 I/O Drive

The 2692 Duart has 7 input only pins and 8 output only pins. The input pins are CMOS gate equivalents, and IP0–3 have change of state detection capabilities. The output pins are CMOS gate equivalents also, but OP4–7 may act as modem control lines and in this mode are open–drain.

1.2.2 Allocation

It was decided that since this device was going to be used (System Architecture), the output port was best employed to drive the D/A converter. The output port drives the D/A (DAC08) directly, although the actual outputs are complements of the output register. Writing has to be performed in two steps, as there are two locations – 1 for setting a bit, 1 for resetting it. Therefore the **MX** software **must** ensure that this process is indivisible. **This may be achieved by writing a word to the register pair.**

The input ports are used for the less important input functions as access to the processor port pins is much better than to the DUART pins (this might require use of the shared interrupt). One input, IP2, is used to get the clock signal into the counter–timer for the MIDI channel. This provides with 4MHz derived from division of the processor's 8MHz CLKOUT signal. The counter–timer must be set to give the 31.25kbaud MIDI frequency.

Four of the input pins are used to detect the status of the memory card (See Functional Description 2.1.4).

PORT PIN	FUNCTION NAME	RESET STATE	COMMENT
IP0	CARD_DET	0	High = Mem Card present
IP1	WP	1	High = Card is write protected
IP2	CLK_BY_4	X	DUART clock for timer/counter (MIDI)
IP3	/POWER_ON	0	Low when power switch is on
IP4	B0	1	Mem. card type bit 0
IP5	B1	1	Mem. card type bit 1
IP6	B2	1	Mem. card type bit 2

Memory Map

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Memory Map

1 GENERAL

The memory map is shown in Fig. 1. The map is divided into code and data spaces with 64kbytes in each. The map has changed from the original specification (Ref. [2]) to give more data space, by compressing the peripheral address space to 1kbyte and the card window to 2kbytes. The code space has been expanded with the bottom 32 kbytes being fixed and the top being paged into 2 equal 32kbyte blocks.

Memory decoding is achieved with 2 GAL20V8–15 devices and a 74AC138 (IC32). The precise details of the GAL encoding is held in the PLD design file S4006001.sds (Ref. [24]).

2 WAIT STATES AND BUSWIDTH

Wait states are controlled with the READY pin. The peripherals and memory card are run in 8 bit mode (BUSWIDTH = 0), with 3 wait states.

The ROM is run in 16 bit mode, wait states are controlled by the ROM_WAIT pin. If ROM_WAIT is high, (default at power up) 1 wait state is inserted. If the unit is a 48 channel one, then the software switches ROM_WAIT to 0 after BIST has been completed. ROM then runs with no wait states. This requires 100nS or faster parts. 0 wait states are not used on the 12/24 for cost reasons, **however, fast EPROMS will work with 12/24 channel systems.**

RAM is generally run with 1 wait state. However, in the protected area (see below), it may be read with 0 waits. Protected RAM contains frequently accessed scene and FX information. Advantage is taken of the fact that RAM timings are faster for reads than writes.

3 MEMORY PROTECTION

MX incorporates extensive memory protection. Attempts to write to ROM cause a non–maskable interrupt (via MEM_CORRUPT) as do attempts to write to the protected area of RAM or the memory card without first asserting /ENABLE_RAM. This means that in the unlikely event of a software upset, the most likely result will be an NMI. The user sees this as a fatal error 1417 "Invalid Interrupt".

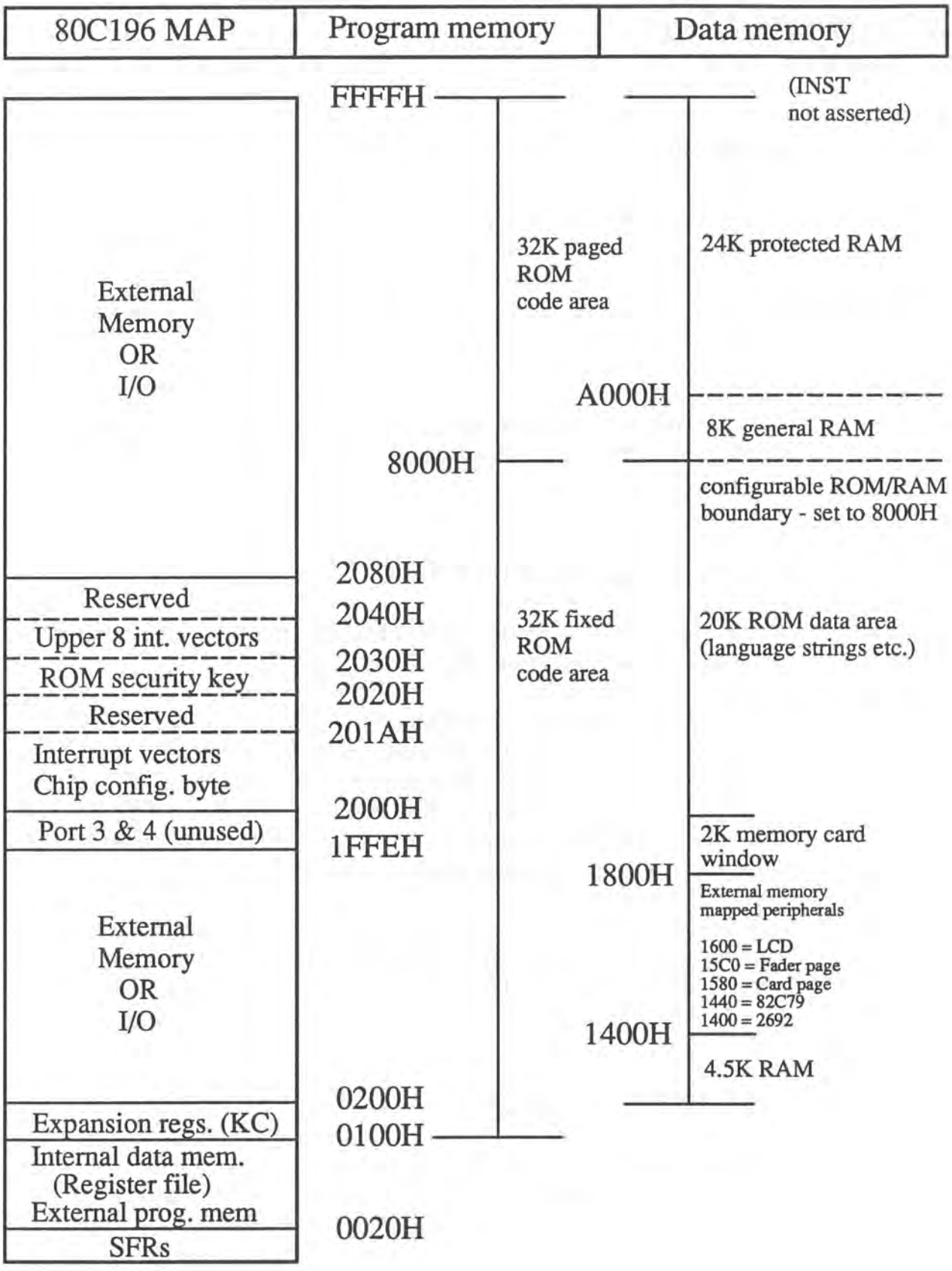

Figure 1 – Memory Map

Test Specification

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Figure 1 Test Jig Arrangement

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Test Specification

1 GENERAL

The MX control PCB software incorporates extensive Built–In– Self Test (BIST) functions and the general philosophy of these is outlined in the Design Specification (1X 33154) and the System Architecture Document (1X 33180). These are resident in the standard product's software, which is the same across all models.

It is required that the control PCB is given an in–circuit– test to detect obvious manufacturing defects before attempting to run any of the BIST tests. It is desirable for the fader PCB to be in–circuit–tested, but not essential.

Both the fader and control PCB's are tested using the control PCB BIST software.

The resident tests may be run in a number of ways, depending on the required procedure, each mode is optimised for that test procedure. The control PCB incorporates 2 test inputs on the test connector (PL5) – these are called M1 and M2. The four possible combinations of these pins give three test modes and the normal user mode. These pins are connected directly to the processor, so require a minimum of hardware to perform. **These pins are only sampled at RESET, so /RESET (available at the test connector) must be asserted briefly when changing modes.**

Additionally, the tests may be run from the menu system on the LCD, the modes are split into SERVICE tests, which require the test jig to be attached, and USER tests, which require no jig. The tests may be run cyclically, to help find spurious failures, during soak test for example.

1.1 Definitions

DMM – Digital Multimeter.

2 OVERVIEW OF TEST FACILITIES

2.1 Test LED

The control PCB incorporates a test LED, which appears on the back panel of a complete unit. The normal sequence of operation for this LED is:

1. A brief flash ON after RESET to indicate that the LED is operational. Failure should be investigated immediately as it means that either the processor is not running, or the LED itself is not working.

2. A short period OFF (approx. 1/2 – 1 secs.) while a small part of the RAM is non–destructively tested. If the LED does not re–illuminate, the RAM is faulty.

3. A short period ON (approx. 1/2 – 1 secs.) while the LCD is tested. If the LED goes off during this period, the LCD is faulty. Having passed the LCD test, the LED should then remain on as long as the unit is powered and not RESET. The system automatically resets on finding RAM or LCD (fatal) errors and therefore keeps re–trying the test sequences.

Having completed the LCD test, the LCD will indicate all further test information.

2.2 Test Modes

The two test connector pins M1 and M2 provide the following tests:

1. M1=0, M2=0 – Mode 0

Birth:

This is the functional test for the complete control PCB before assembly with the control panel. This mode destructively initialises all the data areas in the RAM and does all possible tests in sequence. It is required that all elements of this test are passed before the control PCB is passed to be assembled mechanically with the control panel.

The test jig must be connected to run this test sequence correctly. A part of this jig is also a Gold Brick set of components – four fader PCB's must be connected and a memory card inserted in the card socket. Fig. 1 illustrates the required test jig.

NOTE: The memory card will be formatted during the test procedure, – it must contain no valuable data!

When the test sequence completes, the board goes into normal operating mode.

2. M1=0, M2=1 – Mode 1

Cycle:

In this mode, all tests that require no operator input are run cyclically. The control PCB must have been born and requires the same test jig as Birth above. This mode

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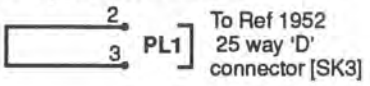
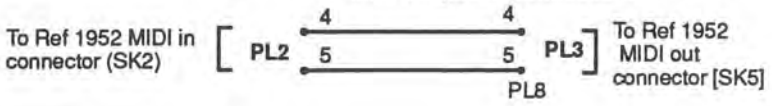
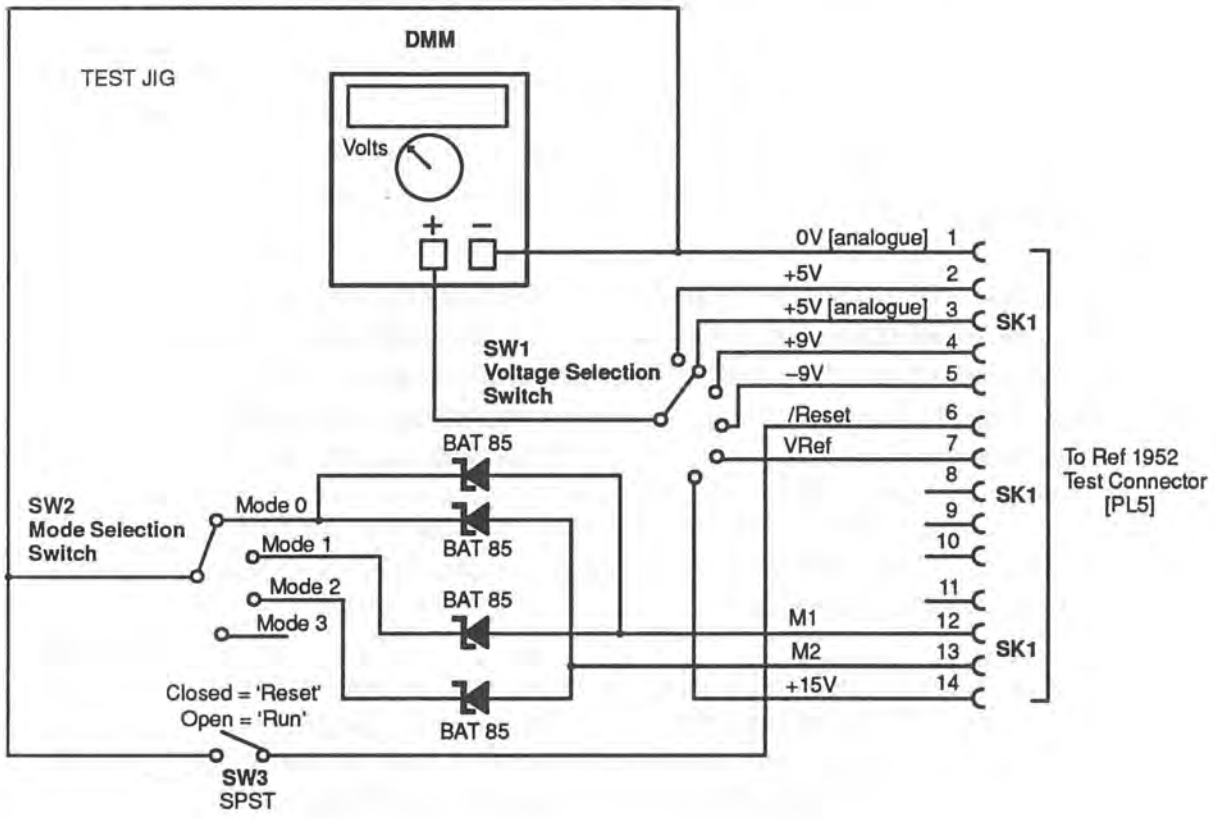
RS 232 Loopback Connections



MIDI Loopback Connections



INTERCONNECTION DETAILS



CONSTRUCTION DETAILS

Test Connector Details

1. ITEMS
   SK1 - 14 way MOLEX socket [0.1"]
   Diodes are all type BAT 85
   SW1 - 1 pole 6 way rotary switch
   SW2 - 1 pole 4 way rotary switch
   SW3 - SPST switch
2. Mount all switches on suitable panel
3. Wire all components as per interconnection details
4. Check all connections with continuity tester
5. Label switches as shown

Loopback Connector Details

1. PL1 is 25 way 'D' type connector [free]
2. PL2, 3 are 5 pin DIN connectors [free]

Figure 1 – Test Jig Arrangement

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is designed to allow extensive testing in environmental chambers and may also be run while cycling the power to the unit to check for memory corruptions etc.

3. M1=1, M2=0 – Mode 2

Fader Test:

In this mode, the unit will only test one or more connected fader PCB's. This requires considerable user input as all switches and faders have to be exercised to pass the test. This mode is provided for use on a gold brick system when just testing fader PCB's.

4. M1=1, M2=1 – Mode 3

Normal:

In this mode, the unit will perform a power–up self test sequence which will be a subset of the BIST functions, but will be invisible to the user unless a fault is found. The fault will then be reported as in the tests above. A single message will normally be displayed telling the user that self tests are in progress. The total time for these tests will depend on whether it is a cold or warm start.

A cold start is performed when the board was last powered down deliberately using the on/off switch. A fairly extensive set of tests are performed and then the board is used as normal.

A warm start is performed when the board was last powered down by a mains failure. A short set of tests are performed to check the integrity of the Scene, FX, Patch and Setup memory and then the board is used as normal. Any running effects or fades continue from their position at power failure.

2.3 Test Procedures

These are split into the three: those for the control PCB, those for the fader PCB, and those for the finished product.

2.3.1 Control PCB

2.3.1.1 Equipment Needed

1. 4 off tested captive fader PCB's (REF 1953) with inter– module ribbon cable.

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2. Test jig (fig. 3).

3. DMM.

2.3.1.2 Procedure

1. After in–circuit–test which should detect opens/shorts, missing, wrong, or reversed components, the current version of MX EPROMS should be installed, even (low order) in socket for IC36, odd (high order) in IC39.

   If it is known that the control PCB is to be part of a 48 way system, the EPROM type should have 100nS or less access time (part no 159/B435). If the system is to be a 12 or 24 way, the EPROMs may have up to 200nS access time (159/B412). Mark the PCB accordingly on the rear.

   The software allows either type of EPROM set to be used for all modes other than NORMAL.

CAUTION!

If a 48 way system is used in NORMAL mode with slow EPROMs, the system will crash after the BIST sequence. This is because the software switches out the EPROM wait states for a 48 way system at this point. A system crash may corrupt the memory, so causing memory corruptions to be registered at the next power up. A BIRTH sequence should be performed if this occurs

---

2. Install the battery link, LK1 if not already installed.

3. Connect the test jig (Fig. 1) including transformer power supply.

4. Set the test mode to 0, set RESET to RESET.

5. Switch on the power using the PCB mounted switch.

6. Check the following voltages with respect to pin 14 of PL5:

Nominal value	Min.	Max.
+15V	14V	24V
+5.1V(nominal 5V)	4.95V	5.25V
+5V_ANL	nominal 5V – 0.2	nominal 5V
+9V	8V	10V
–9V	–10V	–8V
VREF +5.1V	4.95V	5.25V

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7. Switch RESET to RUN

8. The BIST will now start to run. Firstly the test LED should light in the cycle described above, then, as the tests are performed, a banner will appear in the LCD to indicate which test is under way. If a test fails, first **RETRY**, if the test does not pass, turn off the unit and find the fault. Re–do the test procedure until all tests are passed.

NOTE:

a) Some tests are so fast that the banner will not necessarily be seen. Faults will be presented (as an ERROR) with accompanying diagnostic information.

b) Appendix 1 describes each test. The possible errors produced are listed by number.

c) Appendix 2 describes each error, its diagnostic information and an indication as to the possible cause of the fault, and suggested corrective action.

d) The test software is not capable of testing the LCD backlight. If the display does not light up when the RESET is switched to RUN, this fault should be investigated before proceeding.

9. Switch off the unit using the ON/OFF switch and disconnect the two last fader PCB's – so making the system a 24 way.

10. Set the test mode back to **NORMAL.**

11. Switch the unit back on and check that it performs a cold start – ie the banner appears with the words '**Running self test...**'. Check that the display also shows '**MX 24 Version...**' If this does not occur, ie the unit does a warm start, this is indicative of a fault in the power fail circuitry (R51–53 or IC10 or the pf signal itself).

12. Repeat above but this time pull the power plug out, leaving the unit switched on. Re–power the unit and check that a warm start is performed. If a cold start is performed, the /POWER_ON signal is suspect. Switch the unit off using the ON/OFF switch.

13. When all tests have been completed, and passed, remove the test jig, fit the test passed label **and indicate on the label whether fast or slow EPROMS are fitted,** and pass the PCB on for assembly with the control panel. **Note:** EPROM change may be required for final product – see 2.3.3 below.

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14. There are no adjustments or other tests to perform.

2.3.2 Fader PCB

2.3.2.1 Equipment Needed

1. Captive **MX** control PCB (REF 1952) set to run **fader test**, M1=1 M2=0.
2. DMM.

2.3.2.2 Procedure To Test 1–4 Panels Simultaneously

This test procedure can be used for 1–4 fader panels. Panels not connected will not be included in the test cycles. Ideally four panels should be tested together, so that all four positions for SW13 on all PCB's can be tested.

1. Check boards for manufacturing defects.
2. Put all faders at zero, set SW13 on the test panels :

   Panel one to position 1
   Panel two to position 2
   Panel three to position 3
   Panel four to position 4.
3. Connect fader panels to captive **MX** and power up in RESET.
4. Check the power rails with voltmeter w.r.t. ANL_GND at PL1 pin 33:

Nominal Value	min.	max.	Check
+5V_ANL	nominal 5V – 0.2	nominal 5V	check at IC9 pin 16
+9V	8V	10V	check at IC1 pin 7
+5V_LAMPS	nominal 5V – 0.2	nominal 5V	check at emitter of VT2

5. Take control PCB out of reset. LEDs will now be in a short flash sequence:
   1. All LEDs flash on – check for uniformity of brightness.
   2. Single LED on, chasing from LED1 panel 1 to LED12 panel 4 – check for no shorts

6. LEDs will all go on for a short time, then off.

   The LCD will now indicate the flash button to press, (from SW1 panel 1 to SW12 panel 4). On pressing each button, the respective channel LED will indicate acceptance and the LCD will prompt for the next one. A stuck key will be indicated by the respective LED being on and an error message on the LCD. There is an opportunity to re–try the test at this point.

   After SW12 position 4 the next test will start.

7. Take each fader in turn (from VR1 panel 1 to VR24 panel 4) and set to full and back to zero. The LEDs will light for any column with faders not at zero. Check that each fader gives a smooth transition of percentage values, with reaching 1% or less at the bottom, 99% or greater at the top.

8. In order to check that the addressing works for on all PCB's in all positions, do the following three tests. Set SW13 on the test panels :

   Panel one to position 4
   Panel two to position 1
   Panel three to position 2
   Panel four to position 3.

   Set the board to RESET momentarily, and then to RUN.

   Perform test 6 again.

9. Set SW13 on the test panels :

   Panel one to position 3
   Panel two to position 4
   Panel three to position 1
   Panel four to position 2.

   Perform test 6 again.

   Set the board to RESET momentarily, and then to RUN.

10. Set SW13 on the test panels :

    Panel one to position 2
    Panel two to position 3
    Panel three to position 4
    Panel four to position 1.

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Set the board to RESET momentarily, and then to RUN.

Perform test 6 again.

11. If passed test fit tested label to all PCB's.

2.3.3 Finished Product

1. Check that EPROM set is of the correct type. Use 159/B412 type EPROMS for 12/24 way systems, 159/B435 for 48 channel.

2. Connect the power supply and switch the unit on.

3. Check that the unit performs a cold start. If not turn the unit off and on again. Verify that no faults appear during power up tests. Verify that all LEDs illuminate on all fader panels.

4. Connect an EC90 dimmer (set for auto MUX protocol mode) to the D54, DMX and AMX outputs in turn. Using the menu selection SETUP –> IO –> DIMMER, verify that each output works satisfactorily. **Note that EC90 software versions prior to A1 do not support SMX.**

5. Using the Menu system, access the ERROR LOG. Check that there are no entries in the log, if there are, investigate the cause.

6. When power up tests pass, leaving no trace in the error log, access the SETUP CLEAR menu, and choose the WHOLE SYSTEM option, and press CLEAR, followed by YES. This step ensures that the system has default settings for the customer.

7. Verify that a memory card fits into the unit and reads / writes correctly.

2.3.4 Service

MX provides access to most of the tests via the menu system. The operator is provided with both USER and SERVICE type tests. The distinguishing charactaristic is the fact that the jig (fig. 3) has to be used to get error–free results on a good system when executing service tests. All USER tests may be run without the jig. The tests are detailed in Appendix 1.

Appendices

CONTENTS

Appendices

1 APPENDIX 1 – MX SELF TESTS

1.1 Introduction

All tests are performed on the premise that if successful, they will return control to the user without any message. It is therefore assumed that if the given test does not produce an ERROR it is successful. There is no positive indication of "PASS". All test failures are indicated by an ERROR in the format described in this appendix. This appendix lists the tests with the possible ERROR numbers that may be generated.

The following tests are performed on BIRTH, in the order listed:

A TO D REF TEST
FADER CONNECTIONS TEST
RAM TEST
ROM TEST
NMI TEST
CHECK DATA AREAS
A TO D REF TEST
LCD CONTRAST TEST
LCD TEST
D TO A REF TEST
BATTERY TEST
D TO A TEST
D54 SYNC. TEST
RS232 TEST
MIDI TEST
DMX/SMX TEST
AUDIO INPUT TEST
MEMORY CARD TEST
FADER MODULE TEST
CONTROL MODULE TEST

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The following tests are performed on COLD START, in the order listed:

A TO D REF TEST
FADER CONNECTIONS TEST
RAM TEST
ROM TEST
NMI TEST
CHECK DATA AREAS
A TO D REF TEST
D TO A REF TEST
BATTERY TEST
D TO A TEST
D54 SYNC. TEST
RS232 TEST (internal only)
MIDI TEST (internal only)
DMX/SMX TEST
FADER MODULE TEST (LEDs and stuck keys only)
CONTROL MODULE TEST (LEDs and stuck keys only)

The following tests are performed on WARM START, in the order listed:

A TO D REF TEST
FADER CONNECTIONS TEST
CHECK DATA AREAS

The following tests are performed on FADER TEST, in the order listed:

A TO D REF TEST
FADER CONNECTIONS TEST
FADER MODULE TEST
<repeat>

The following tests are performed on CYCLE TEST, in the order listed:

FADER CONNECTIONS TEST
RAM TEST
ROM TEST
NMI TEST
CHECK DATA AREAS
A TO D REF TEST
LCD CONTRAST TEST
LCD TEST
D TO A REF TEST
BATTERY TEST
D TO A TEST
D54 SYNC. TEST
RS232 TEST
MIDI TEST
DMX/SMX TEST
AUDIO INPUT TEST

MX

MEMORY CARD TEST
FADER MODULE TEST
CONTROL MODULE TEST
<repeat>

However no parts of the tests requiring user input (faders, keys etc) are executed. Tests do not report errors on screen, these may be viewed in the error log.

1.2 Test Descriptions

ROM TEST

This test checks the data part of the EPROM set. Due to the 80C196 architecture, it is not possible to check the code part of the ROM. However, any EPROM problems will probably be highlighted by this test.

Possible errors: 1390

RAM TEST

This test non–destructively tests the RAM, ie writes patterns to the RAM, testing each bit in turn.

Possible errors: 1389

NMI TEST

This test checks that a Non–Maskable interrupt is seen when an attempt is made to write to an area of protected memory. There are 3 areas – the data areas, the memory card and the EPROM.

Possible errors: 1391

CHECK DATA AREAS

This test checks the integrity of the protected data areas, by verifying their checksums.

Possible errors: 1384, 1385, 1386, 1387

FADER CONNECTIONS TEST (at every power–up)

This test checks that a valid set of fader modules are connected to the control PCB.

Possible errors: 1388

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LCD TEST

This test invokes the LCD CONTRAST TEST. Having done this it puts all segments of the LCD on for the user to check visually.

Possible errors: 1393

LCD CONTRAST TEST

This test checks that the LCD contrast can be controlled by the processor. It changes the contrast between max. and min, checking the LCD reference voltage.

Possible errors: 1393

A TO D REF TEST (at every power up)

This test checks that the A/D reference (set by two equal resistors R95, 96) is reading 2.6V A/D (+/– 10%).

Possible errors: 1392

BATTERY TEST

This test checks that the back-up battery is within tolerance. Also tests measuring circuit, giving indication of possible A/D problems.

Possible errors: 1395, 1396

D TO A REF TEST

This test checks the D/A reference generator by setting it to a known value and checking against the A/D.

Possible errors: 1394

D TO A TEST

Having performed a test to ascertain full–scale on the D/A, this test checks the D/A by setting each bit in turn and checking it against the A/D.

Possible errors: 1397

D54 SYNC. TEST

This test checks that the processor has full control of the D/A and associated circuitry. It generates a voltage with the D/A and checks that the D54 sync. pulse can be correctly superimposed. It also checks that the D/A can be enabled / disabled.

Possible errors: 1398

MX

RS232 TEST(internal)

This test checks that RS232 part of the DUART (IC25) is working correctly by sending / receiving a stream of data internally.

Possible errors: 1399

RS232 TEST (external)

This test checks that RS232 part of the DUART (IC25) is working correctly by sending / receiving a stream of data externally using the interface ICs. It therefore requires a physical loopback on the 25 pin D type between pins 2 & 3

Possible errors: 1400

MIDI TEST (internal)

This test checks that MIDI part of the DUART (IC25) is working correctly by sending / receiving a stream of data internally.

Possible errors: 1401

MIDI TEST (external)

This test checks that MIDI part of the DUART (IC25) is working correctly by sending / receiving a stream of data externally using the interface ICs. It therefore requires a physical loopback between the MIDI IN and MIDI OUT

Possible errors: 1402

DMX/SMX TEST

This test checks that RS 485 port is working correctly by sending / receiving a stream of data externally using the interface ICs. No loopback is required, but it is necessary to ensure that there is no significant load on the port.

Possible errors: 1403

AUDIO INPUT TEST

This is a complex test. It requires the AUDIO/MIDI fader to be set to full to operate successfully. This is tested before the actual audio input is tested. An incorrect setting will give error 404. A series of tone bursts, at increasing frequency and low level, are then generated by the processor. These are fed into the audio processor, which should generate appropriate interrupts.

Possible errors: 404, 1405

MX

MEMORY CARD TEST

BEWARE: This test requires a memory card and will FORMAT it, so destroying any valuable data held.

This test does two things. First, it attempts to create a file on the card called TEST.BIN (The card is MS–DOS formatted). Having created this file, it checks it for integrity. In the second part of the test it writes a pattern of bytes into the 32 pages of the card (64 kbyte) to check that the card page register is working correctly.

Possible errors: 320, 322, 324, 325, 326, 336, 337, 338, 1321, 1323, 1406, 1407

FADER MODULE TEST

This test has a number of sub–tests. The first is a sequence through the flash LEDs, followed by all on. Next, the LCD prompts the user to press each flash key in turn. The associated LED will light in each case. Finally, the LCD prompts the user to cycle each fader in turn through its full travel. A full excursion is required in each case. The percentage level is displayed on the LCD. The user should check for acceptable performance. The faders must all be at 0 before starting this test.

Possible errors: 1408, 1409

CONTROL MODULE TEST

This test has a number of sub–tests. The first is a 'build' through the control PCB LEDs. Next, the LCD prompts the user to press each named key in turn. Finally, the LCD prompts the user to cycle each fader in turn through its full travel. A full excursion is required in each case. The percentage level is displayed on the LCD. The user should check for acceptable performance. The faders must all be at their 0 positions before starting this test.

(Faders set away from front: TIME A, TIME B, B MASTER , D MASTER, FX FADE TIME, FX STEP TIME. All others set nearest front)

Possible errors: 1410, 1411, 1412

MX

2 APPENDIX 2 – ERROR MESSAGES

This Appendix describes all possible errors that MX can generate.

2.1 Introduction

All ERROR's are reported in a uniform way using MX's central error handler and the LCD display.

The format is always:
— ERROR #### — (#### is the error number)
Ident. string
Diagnostic info.
PROMPT

Each error is allocated a unique number and identification string as a brief description. Depending on the type of error, some diagnostic information may be presented. This varies in type depending on the error, and is described below.

The user is prompted with the soft key labels at the bottom of the screen, or if the error is Fatal (ie the system cannot continue with such a serious fault), the user is warned that the system is about to RESET itself with the string: "Resetting system!"

Error numbers appear in two types:

Those with numbers less than 1000 are generally of a less serious nature and are not logged.

Errors with numbers greater than 1000 are regarded as serious and are logged in the internal ERROR LOG. The log is for both user and service purposes, and allows the last 100 errors to be viewed.

The errors are not consecutively numbered because each number comprises:

The software module where the error was generated.

The error number within that module.

Some errors, particularly those that are likely to be seen by the user (for example when a memory card transfer is attempted with no card in place), are translated into the 3 languages supported. Test and system type errors are only presented in English.

There are 3 types of general diagnostic data:

1) Voltages:
These are presented as a result of internal tests in the form:
X.XX Y.YY Z.ZZ, where X is the voltage read, Y is the highest voltage and Z is the lowest voltage allowed.

2) Addresses/Data:
These are presented in the form HHHH, where H is a hexadecimal number.

3) Fader levels:
These are presented as AAA, where A is the percentage of full travel as read from the fader in question.

Other forms of data may be used – these are described in individual cases.

2.2 Error Descriptions

ERROR	12
Identification:	"Record Inhibited!"
Diagnostic Information:	None
Type:	System/Warning
Description:	Record lock is activated, disallowing record/modify actions
Probable cause:	
Remedy:	Turn RECORD/LOCK to OFF

ERROR	288
Identification:	"MIDI framing error"
Diagnostic Information:	None
Type:	MIDI interface/Warning
Description:	A byte of MIDI data was received with incorrect format
Probable cause:	Faulty MIDI connections or MIDI cable too long
Remedy:	Find fault or shorten cable

ERROR	289
Identification:	"MIDI RX overrun"
Diagnostic Information:	None
Type:	MIDI interface/Warning
Description:	A byte of MIDI data was received before the last was processed
Probable cause:	MIDI data was transmitted to MX too fast. or MIDI data transmitted to MX during test
Remedy:	Reduce amount of MIDI data transmitted to MX or disconnect MIDI device.

ERROR	320
Identification:	"Card full"
Diagnostic Information:	File name accessed
Type:	Memory Card/Warning
Description:	The memory card is full.
Probable cause:	There is insufficient room to save data to the memory card.
Remedy:	Delete DOS files not used by MX, or FORMAT card.

ERROR	322
Identification:	"Card missing!"
Diagnostic Information:	Filename accessed
Type:	Memory Card/Warning
Description:	The memory card is not inserted correctly
Probable cause:	
Remedy:	Insert card, try again.

ERROR	324
Identification:	"Card write protected"
Diagnostic Information:	Filename accessed
Type:	Memory Card/Warning
Description:	The card is write protected and may not have data saved on it
Probable cause:	The card write protection switch is set to ON
Remedy:	Confirm that you wish to overwrite data, then change write protection to OFF and re–try

ERROR	325
Identification:	"Invalid card format"
Diagnostic Information:	Filename accessed
Type:	Memory Card/Warning
Description:	The card is not MS–DOS formatted, so may not be used yet
Probable cause:	The card is new, or data has been lost due to battery failure
Remedy:	Use FORMAT to initialize the card

ERROR	326
Identification:	"Card directory full"
Diagnostic Information:	Filename accessed
Type:	Memory Card/Warning
Description:	The card directory has insufficient room for MX data files
Probable cause:	The card may only contain 8 files, MX needs 4 spare entries
Remedy:	Delete DOS files not used by MX, or FORMAT card

ERROR	336
Identification:	"Card file error"
Diagnostic Information:	Filename accessed
Type:	Memory Card/Warning
Description:	The software has detected a fault in the MX card file read
Probable cause:	The card data has been partially corrupted
Remedy:	QUIT card reading

MX

ERROR	337
Identification:	"Card file closed"
Diagnostic Information:	Filename accessed
Type:	Memory Card/Warning
Description:	The software has detected a fault in the MX card file read
Probable cause:	The card file has been edited in some way
Remedy:	QUIT card reading

ERROR	338
Identification:	"Card file missing"
Diagnostic Information:	Filename accessed
Type:	Memory Card/Warning
Description:	The card file requested was not found on the card
Probable cause:	The card does not contain the requested data
Remedy:	QUIT card reading

ERROR	339
Identification:	"Partial Transfer"
Diagnostic Information:	Filename accessed
Type:	Memory Card/Warning
Description:	The card file requested was only partially saved or read
Probable cause:	There was a fault in the data, and the transfer was QUITTED
Remedy:	Try again, use CONTINUE to finish reading card data

ERROR	352
Identification:	"RS232 framing error"
Diagnostic Information:	None
Type:	RS232 interface/Warning
Description:	A byte of RS232 data was received with incorrect format
Probable cause:	Format of data transmitted to MX is different to SETUP RS232
Remedy:	Check format of data transmitted and change either MX or remote device SETUP accordingly

ERROR	353
Identification:	"RS232 RX overrun"
Diagnostic Information:	None
Type:	RS232 interface/Warning
Description:	A byte of RS232 data was received before the last was processed
Probable cause:	RS232 data was transmitted to MX too fast. or data transmitted to MX during test
Remedy:	Reduce baud rate or disconnect RS232 device.

ERROR	354
Identification:	"RS232 parity error"
Diagnostic Information:	None
Type:	RS232 interface/Warning
Description:	A byte of RS232 data was received with incorrect parity
Probable cause:	Remote devices' RS232 data SETUP was different to MX, faulty connections present, or cable too long
Remedy:	Change EITHER MX OR remote device SETUP accordingly, find bad connection or shorten cable

ERROR	404
Identification:	"Audio fader too low"
Diagnostic Information:	% level read, valid max / min % levels
Type:	Test/Warning
Description:	The audio fader is set too low for the audio input test
Probable cause:	Fader set incorrectly
Remedy:	Set audio fader to full (10)

ERROR	1001
Identification:	"No such handle!"
Diagnostic Information:	None
Type:	System/Fatal
Description:	The system has attempted to access a non–existent "device".
Probable cause:	Program fault
Remedy:	System reset

ERROR	1002
Identification:	"No such read!"
Diagnostic Information:	None
Type:	System/Fatal
Description:	The system has attempted to access a non–existent "device".
Probable cause:	Program fault
Remedy:	System reset

ERROR	1003
Identification:	"No such write!"
Diagnostic Information:	None
Type:	System/Fatal
Description:	The system has attempted to access a non–existent "device".
Probable cause:	Program fault
Remedy:	System reset

ERROR	1004
Identification:	"Null Ptr used!"
Diagnostic Information:	None
Type:	System/Fatal
Description:	The system has attempted to access a non–existent string or function.
Probable cause:	Program fault
Remedy:	System reset

ERROR	1005
Identification:	"Circ buffer full!"
Diagnostic Information:	None
Type:	System/Warning
Description:	The system has run out of space in a data buffer
Probable cause:	Too much data being transmitted to MX or I/O device fault
Remedy:	Reduce amount data being transmitted or investigate fault

ERROR	1006
Identification:	"Invalid parameter!"
Diagnostic Information:	None
Type:	System/Fatal
Description:	Invalid information was sent to a data buffer
Probable cause:	Program fault
Remedy:	System reset

ERROR	1007
Identification:	"Watchdog timed out!"
Diagnostic Information:	Module number
Type:	System/Fatal
Description:	A watchdog timer has expired.
Probable cause:	Program fault or system overloaded in some way
Remedy:	System reset

ERROR	1008
Identification:	"Bad interrupt!"
Diagnostic Information:	Interrupt number (HEX)
Type:	System/Fatal
Description:	An unexpected/unused interrupt was received.
Probable cause:	Program or processor fault, probably due to noisy environment
Remedy:	System reset

ERROR	1009
Identification:	"Duplicate string!"
Diagnostic Information:	None
Type:	System/Fatal
Description:	A duplicate string was found whilst initializing the hash table
Probable cause:	EPROM fault
Remedy:	Replace EPROM set

ERROR	1010
Identification:	"No such open!"
Diagnostic Information:	None
Type:	System/Fatal
Description:	The system has attempted to access a non–existent "device"
Probable cause:	Not used
Remedy:	

ERROR	1011
Identification:	"Power fail stuck!"
Diagnostic Information:	None
Type:	System/Fatal
Description:	The power fail signal is stuck in its active state or power on signal absent.
Probable cause:	Inter–PCB cable faulty, PSU chip failure or switch faulty.
Remedy:	Find and correct fault.

ERROR	1192
Identification:	"LED – I/O fault"
Diagnostic Information:	None
Type:	System/Fatal
Description:	The LED controller is not responding to commands
Probable cause:	2MHz clock failure or failure of IC20
Remedy:	Check clock and IC20

ERROR	1224
Identification:	"LCD I/O fault"
Diagnostic Information:	None
Type:	System/Fatal
Description:	The LCD is not responding to commands.
Probable cause:	LCD cable or LCD controller failure.
Remedy:	Find and correct fault.

ERROR	1225
Identification:	"LCD – invalid ansi"
Diagnostic Information:	None
Type:	System/Fatal
Description:	An attempt was made to write a non–ansi symbol to the LCD
Probable cause:	Program fault
Remedy:	System reset

ERROR	1226
Identification:	"LCD – invalid pos"
Diagnostic Information:	None
Type:	System/Fatal
Description:	An attempt was made to write to an invalid position on the LCD
Probable cause:	Not used
Remedy:	

ERROR	1321
Identification:	"Card R/W error"
Diagnostic Information:	File written
Type:	Memory Card/Warning
Description:	The data written to the card was not verified correctly
Probable cause:	Faulty memory card or card interface circuitry
Remedy:	Try again, if error persists, replace card and/or service MX

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ERROR	1323
Identification:	"Card battery low"
Diagnostic Information:	File name accessed
Type:	Memory Card/Warning
Description:	The card battery voltage is too low for reliable operation
Probable cause:	The card battery has fallen below 2.6V and is exhausted
Remedy:	Replace Memory card battery – see repair handbook for details

ERROR	1384
Identification:	"Scene corrupt!"
Diagnostic Information:	Scene in format Pg.Scene
Type:	Test/Warning
Description:	A scene checksum has failed
Probable cause:	Internal battery discharged, or mem. card battery exhausted, or power fail detection circuitry faulty
Remedy:	Press CONTINUE to clear the scene, or, if performing memory card transfer, press CONTINUE to carry on after ignoring scene or QUIT to end the transfer.

ERROR	1385
Identification:	"Effect corrupt!"
Diagnostic Information:	Effect in format Pg.Effect
Type:	Test/Warning
Description:	An Effect checksum has failed
Probable cause:	Internal battery discharged, or mem. card battery exhausted or power fail detection circuitry faulty
Remedy:	As error 1384

ERROR	1386
Identification:	"Setup corrupt!"
Diagnostic Information:	None
Type:	Test/Warning
Description:	The setup checksum has failed
Probable cause:	Internal battery discharged, or mem. card battery exhausted or power fail detection circuitry faulty
Remedy:	CONTINUE or QUIT – cause setup to be reset to factory defaults

ERROR	1387
Identification:	"Patch corrupt!"
Diagnostic Information:	Patch number (1 or 2)
Type:	Test/Warning
Description:	A dimmer patch checksum has failed
Probable cause:	Internal battery discharged, or mem. card battery exhausted or power fail detection circuitry faulty
Remedy:	As error 1384

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ERROR	1388
Identification:	"Fader module fault"
Diagnostic Information:	Module code
Type:	Test/Fatal
Description:	A fault has been detected in the fader module connections
Probable cause:	Fader module cable fault or invalid id switch combination
Remedy:	Find fault and check switch settings

ERROR	1389
Identification:	"RAM test failed"
Diagnostic Information:	Address, byte read, byte written
Type:	Test/Fatal
Description:	A RAM test pattern has read back incorrectly
Probable cause:	Backup battery low or RAM faulty
Remedy:	Find fault or allow battery to charge

ERROR	1390
Identification:	"ROM checksum failed"
Diagnostic Information:	Checksum read, correct checksum
Type:	Test/Fatal
Description:	The ROM checksum does not agree with the programmed value
Probable cause:	EPROM faulty
Remedy:	Replace EPROM set.

ERROR	1391
Identification:	"NMI fault"
Diagnostic Information:	Address of byte written to stimulate NMI
Type:	Test/Fatal
Description:	An NMI was not seen by the processor when stimulated
Probable cause:	PLD device IC28 incorrectly programmed or faulty.
Remedy:	Find fault or replace IC28.

ERROR	1392
Identification:	"A/D Reference fault"
Diagnostic Information:	Voltage read, max., min. valid voltages
Type:	Test/Warning
Description:	The A/D converter is out of spec.
Probable cause:	R95/96 incorrect or IC26 faulty
Remedy:	Find fault or replace IC26.

ERROR	1393
Identification:	"LCD contrast fault"
Diagnostic Information:	Voltage read, max., min. valid voltages
Type:	Test/Warning
Description:	The LCD contrast control not working correctly.
Probable cause:	VT10, R70, 73, 76, or C64 faulty
Remedy:	Find fault

MX

ERROR	1394
Identification:	"D/A Reference fault"
Diagnostic Information:	Voltage read, max., min. valid voltages
Type:	Test/Warning
Description:	The D/A converter reference is out of spec.
Probable cause:	Inter–PCB cable faulty or D_A_SET signal not present
Remedy:	Find fault

ERROR	1395
Identification:	"Battery volts fault"
Diagnostic Information:	Voltage read, max., min. valid voltages
Type:	Test/Warning
Description:	The battery voltage is out of spec.
Probable cause:	Battery discharged or faulty, Inter–PCB cable faulty
Remedy:	Find fault, or charge battery for several hours, if error persists replace battery.

ERROR	1396
Identification:	"Battery ref fault"
Diagnostic Information:	Voltage difference read, max., min. valid voltages
Type:	Test/Warning
Description:	The battery reference voltage is out of spec.
Probable cause:	R60 faulty, IC18 faulty, A/D faulty (excessive leakage)
Remedy:	Find fault

ERROR	1397
Identification:	"D to A fault"
Diagnostic Information:	EITHER:Voltage read, max., min. valid voltages OR:PWM setting, valid max., min settings
Type:	Test/Warning
Description:	D/A converter is out of spec.
Probable cause:	IC6, IC4, IC7 or associated components faulty, Inter–PCB cable faulty, or IC25 faulty.
Remedy:	Find fault

ERROR	1398
Identification:	"D54 sync. fault"
Diagnostic Information:	Voltage read, max., min. valid voltages
Type:	Test/Warning
Description:	EITHER:The D54 synchronisation pulse is not being generated. OR: The D/A converter ENABLE control is not working.
Probable cause:	R21, 22, D6, Inter–PCB cable faulty, IC6 or IC26 faulty.
Remedy:	Find fault

MX

ERROR	1399
Identification:	"RS232 int–loop fault"
Diagnostic Information:	Byte read, byte written
Type:	Test/Warning
Description:	The internal loopback in IC25 for the RS232 port is faulty
Probable cause:	Memory decoding faulty (IC28, 32) or IC25 faulty, or data being transmitted to MX during test
Remedy:	Find fault, or disconnect RS232 device

ERROR	1400
Identification:	"RS232 ext–loop fault"
Diagnostic Information:	Byte read, byte written
Type:	Test/Warning
Description:	The external loopback for the RS232 port is faulty
Probable cause:	No loopback connector installed?, IC5 faulty
Remedy:	Fit loopback or find fault

ERROR	1401
Identification:	"MIDI int–loop fault"
Diagnostic Information:	Byte read, byte written
Type:	Test/Warning
Description:	The internal loopback in IC25 for the MIDI port is faulty
Probable cause:	4MHz clock failure, Memory decoding faulty (IC28, 32), IC25 faulty or MIDI data being transmitted to MX during test
Remedy:	Find fault or disconnect external MIDI device

ERROR	1402
Identification:	"MIDI ext–loop fault"
Diagnostic Information:	Byte read, byte written
Type:	Test/Warning
Description:	The external loopback for the MIDI port is faulty
Probable cause:	No loopback connector installed?, IC5 faulty
Remedy:	Fit loopback or find fault

ERROR	1403
Identification:	"SMX/DMX port fault"
Diagnostic Information:	Byte read, byte written
Type:	Test/Warning
Description:	The DMX/SMX port loopback is not responding.
Probable cause:	Short on RS485 lines, IC9, IC3 faulty
Remedy:	Find fault

ERROR	1405
Identification:	"Audio test fault"
Diagnostic Information:	Frequency at which test failed
Type:	Test/Warning
Description:	The audio threshold detector has not seen signals at the required test frequencies.
Probable cause:	Wrong components around IC2, IC4, or audio source connected during test
Remedy:	Re–try, find fault., or remove audio source

ERROR	1406
Identification:	"Memory card error"
Diagnostic Information:	Byte read, byte written
Type:	Test/Warning
Description:	The memory card has not read back the test values written
Probable cause:	Connector problem, card interface circuitry problem
Remedy:	Find fault, try another card

ERROR	1407
Identification:	"Mcard paging fault"
Diagnostic Information:	Page number accessed
Type:	Test/Warning
Description:	The memory card has not read back the test values written
Probable cause:	Wrong size card used (64kbyte required) or IC41 faulty
Remedy:	Find fault, try another card

ERROR	1408
Identification:	"Flash key stuck"
Diagnostic Information:	Corresponding channel number
Type:	Test/Warning
Description:	A flash key is stuck in the "on" state
Probable cause:	Key damaged, corresponding pull–up resistor disconnected, or something resting on key during power–up sequence
Remedy:	Find fault

ERROR	1409
Identification:	"Channel fader stuck"
Diagnostic Information:	Corresponding channel number
Type:	Test/Warning
Description:	An A or B preset fader is set at the wrong level
Probable cause:	Faders not reset prior to fader test.
Remedy:	Reset fader!

MX

ERROR	1410
Identification:	"Control key stuck"
Diagnostic Information:	Key number
Type:	Test/Warning
Description:	A control module key is stuck in the "on" state
Probable cause:	Key damaged, corresponding pull–up resistor disconnected, or something resting on key during power–up sequence
Remedy:	Find fault

ERROR	1411
Identification:	"Control key bounced"
Diagnostic Information:	Key name
Type:	Test/Warning
Description:	A control module key has "bounced"
Probable cause:	Key damaged
Remedy:	Find fault or replace key

ERROR	1412
Identification:	"Control fader stuck"
Diagnostic Information:	Fader number, fader expected, % level read
Type:	Test/Warning
Description:	A control fader is set at the wrong level
Probable cause:	Faders not reset prior to fader test.
Remedy:	Reset fader!

ERROR	1416
Identification:	"Watchdog timed out!"
Diagnostic Information:	Module number
Type:	System/Fatal
Description:	A watchdog timer has expired.
Probable cause:	Program fault or system overloaded in some way
Remedy:	System reset

ERROR	1417
Identification:	"Invalid interrupt!"
Diagnostic Information:	Interrupt number (HEX)
Type:	System/Fatal
Description:	An unexpected interrupt was received.
Probable cause:	Program fault, probably due to noisy environment
Remedy:	System reset

MX

3 APPENDIX 3

This Appendix describes the procedure for changing surface mount components

3.1 Introduction

On MX, since the Control PCB REF 1952 is being in–circuit–tested, there should be no need to re–work components. However, just in case ...

The removal and replacement of surface mount components is a specialist skill which takes some practice to acquire.

The following gives an outline of the correct procedure, which should be practiced on an old/unused PCB.

3.1.1 Suitable Tools and Equipment

- Surface Mount Cutters kit STC Components Stock No. 031676R
  or

  Surface Mount heat re–flow station – Circuit Plating Ltd System 1000 Reflow Station.
- Surface mount pick and place machine – Fritsch LM900.500
- Hot air jet
- Tempilaq Temperature indicating fluid.

3.1.2 Removal of Small Surface Mount Components.

Apply heat to all contacts of the component using a Hot air jet. When solder is molten remove component with tweezers.

Apply a small amount of Surface Mount Re–work flux and remove excess solder with solder braid. Be careful not to apply too much heat or force so as to not lift or damage any of the pads on the PCB.

Note: Most of the integrated circuits used on the card are sensitive to ESD (Electrostatic discharge). ESD can permanently damage, or reduce the working life of these components.

Therefore they should only be handled and fitted in an ESD controlled environment. Earthed wrist straps, earthed soldering iron tips and storage of static

sensitive devices in conductive sleeves provides the minimum ESD controlled environment required.

3.1.3 Removal of Integrated Circuits Using Cutters

Probably the easiest way to remove faulty integrated circuits is to snip the legs of the IC and then remove the legs left on the pcb with a small tipped soldering iron.

Select a pair of cutters from the kit with small cutting edges that will fit around the top of the IC leg. Snip the legs near the top, to avoid risk of damaging the PCB pads or tracks. When all legs have been cut then use a soldering iron to remove the remaining legs. This is best done by gently wiping the soldering iron tip across the remaining legs. These will then tend to collect on the tip where they can be removed.

Apply a small amount of Surface Mount Re–work flux and remove excess solder with solder braid. Be careful not to apply too much heat or force so as to lift or damage any of the pads on the PCB.

3.1.4 Removal of Integrated Circuits Using Heat Re–flow Station

Switch on Heat reflow station. Fit a component mask to the both top and bottom heat jets appropriate to the shape of the IC being removed. This ensures heat applied is confined to this area.

Measure/Adjust temperature of reflow station to above the melting point of the solder paste (about 250 degrees C).

Apply Tempilaq Temperature Indicator fluid (degrees C) or similar to each edge of the chip, (remember to shake the bottle well!)

Place PCB into pcb guides (adjust if necessary) and centre on component to be removed.

Move both top and bottom hot air flows into position. They should be immediately above and below component to be removed.

When the temperature indicator fluid has changed colour, quickly move top and bottom jets back into the rest position and remove component with a pair of tweezers.

Parts of the reflow station and the PCB will be **very hot – BE CAREFUL!**

Apply a small amount of Surface Mount Re–work flux and remove excess solder with solder braid. Be careful not to apply too much heat or force so as to lift or damage any of the pads on the PCB.

MX

Replacement of Surface mount components.

Surface mount components may be replaced by using a reflow station or by using a fine soldering iron and fine solder. Each method is described separately.

3.1.5 Replacing Components Using Heat Re–flow Station

Remove Solder paste from cold storage and store at room temperature for several hours before work commences.

Set PICK and PLACE machine regulator pressure to about 35 PSI.

Adjust solder paste dispense time to approx 300ms (030 on the thumbwheel switches).

Fit PCB into upper slots of the XY table, adjusting movable gate against PCB and tighten the gate retaining screw.

Fit Solder paste onto XY head. Move solder dispenser into dispense position by pressing black button on XY head.

Move the XY position control to centre the solder dispenser above component pad. Gently pull down XY control until solder is automatically dispensed onto component pad. Release XY control and move to next PAD, repeat until all components pad have solder paste applied.

Note: Movement in either the X or Y direction can be locked by pressing either the **X** or **Y** button to assist application of the paste.

Move XY control to position the vacuum pick–up nozzle above component to be fitted. Gently pull down the XY control placing the XY nozzle on top of the centre of the component. The machine will automatically use a vacuum to pick up the component.

Note: It is a good idea at this stage to turn on the XY hold function. This will lock movement of the component when it has been placed in position, to prevent the operator dragging it through the solder paste when releasing the IC.

Move the component into position carefully lining up the component with the PCB pads. Gently pull down on the XY control until the component is placed into position. The machine will automatically release the vacuum.

3.1.6 Re–flow Soldering

Switch on Heat reflow station. Fit a component mask to the both top and bottom heat jets appropriate to the shape of the IC being removed. This ensures heat applied is confined to this area.

MX

Measure/Adjust temperature of reflow station to above the melting point of the solder paste (about 250 degrees C).

Apply Tempilaq Temperature Indicator fluid (degrees C) or similar to each edge of the chip, (remember to shake the bottle well!)

Place PCB into pcb guides (adjust if necessary) and centre on component to be removed.

Move both top and bottom hot air flows into position. They should be immediately above and below component to be removed.

When the temperature indicator fluid has changed colour, check that the solder has flowed well by inspecting the soldered pins/pads. If all is well then move top and bottom jets back into the rest position and remove the PCB .

Parts of the reflow station and the PCB will be **very hot – BE CAREFUL!**

3.1.7 Component Replacement Using Soldering Iron

Surface mount components may be fitted to the PCB using a fine tipped soldering iron and fine solder. The following items are suitable for this method;

Weller EC2002D soldering iron fitted with fine tip.

Farnell Stock No. EC2002D

26 SWG solder eg RS 561–101 or Farnell SMART26 solder.

Carefully apply soldering iron to heat both the PCB pad and the component leg. Apply solder to soldering iron tip, allowing solder to flow onto both the component leg and PCB pad. Inspect each solder joint paying particular attention to dry solder joints and fine solder bridges. Rework any joints as necessary.

MX

Drawings

CONTENTS

MX

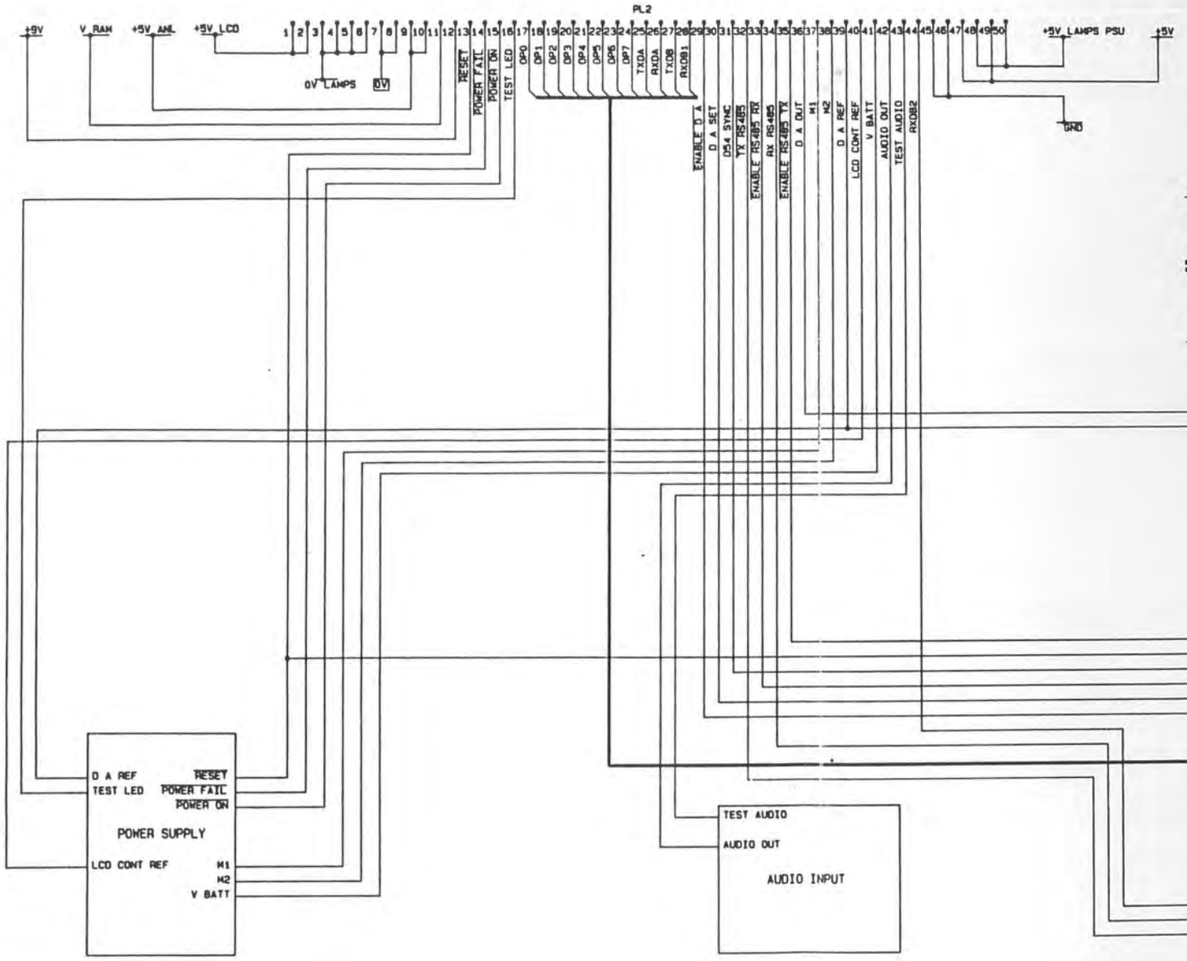
DRG. No.	SH.	ISSUE
68 40045	OF 8	1

3RD ANGLE PROJECTION

DO NOT SCALE IF IN DOUBT-ASK

IC TABLE FOR REACT PSU SECTION.

COMP. REF.	TYPE	Vcc	GND
IC1	H11L1	-	-
IC2	NE571D	-	-
IC3	74AC14SC	14	7
IC4	TL084CD	-	-
IC5	SN751550	-	4
IC6	DAC08-ED	-	-
IC7	LM6321N	-	-
IC8, 9	SN7517680	8	5
IC10	L4963	-	-
IC11, 12	MC7809CT	-	-



SCHEDULE : 5S33219
DRILLING : 5840174

NOTE: ANALOGUE GND = 0V
DIGITAL GND = GND

ISSUES	
PROTOTYPE	
PRE-PROD*	
PRODUCTION	

C.No.
REV. I.

SCALE
DIMENSIONS IN mm
TOLERANCES
1 DEC. PLACE ± 0.4 mm
2 DEC. PLACES ± 0.1 mm
ANGULAR ± 0.25°
UNLESS OTHERWISE STATED

		DATE
DRAWN	R.F.	12/12/89
CHECK'D	K C YOUNG	6/8/90
APP'D		7/9/90

Strand Lighting Ltd
Head Office: Unit 1, Centaurus Business Park, Grant Way, Isleworth, Middlesex TW7 5QD
Tel. 01 560 3171 Telex. 27874 Fax. 01 568 2102
Factory: Manchester Industrial Estate, Eatonside, Fax. KY1 3LY
Tel. 0563 53333 Telex. 73300 Fax. 0563 53638

MATERIAL:-

FINISH:-

TITLE
REACT MAIN PANEL CARD
(PSU BLOCK DIAGRAM)

PCB1014/1 REF1952

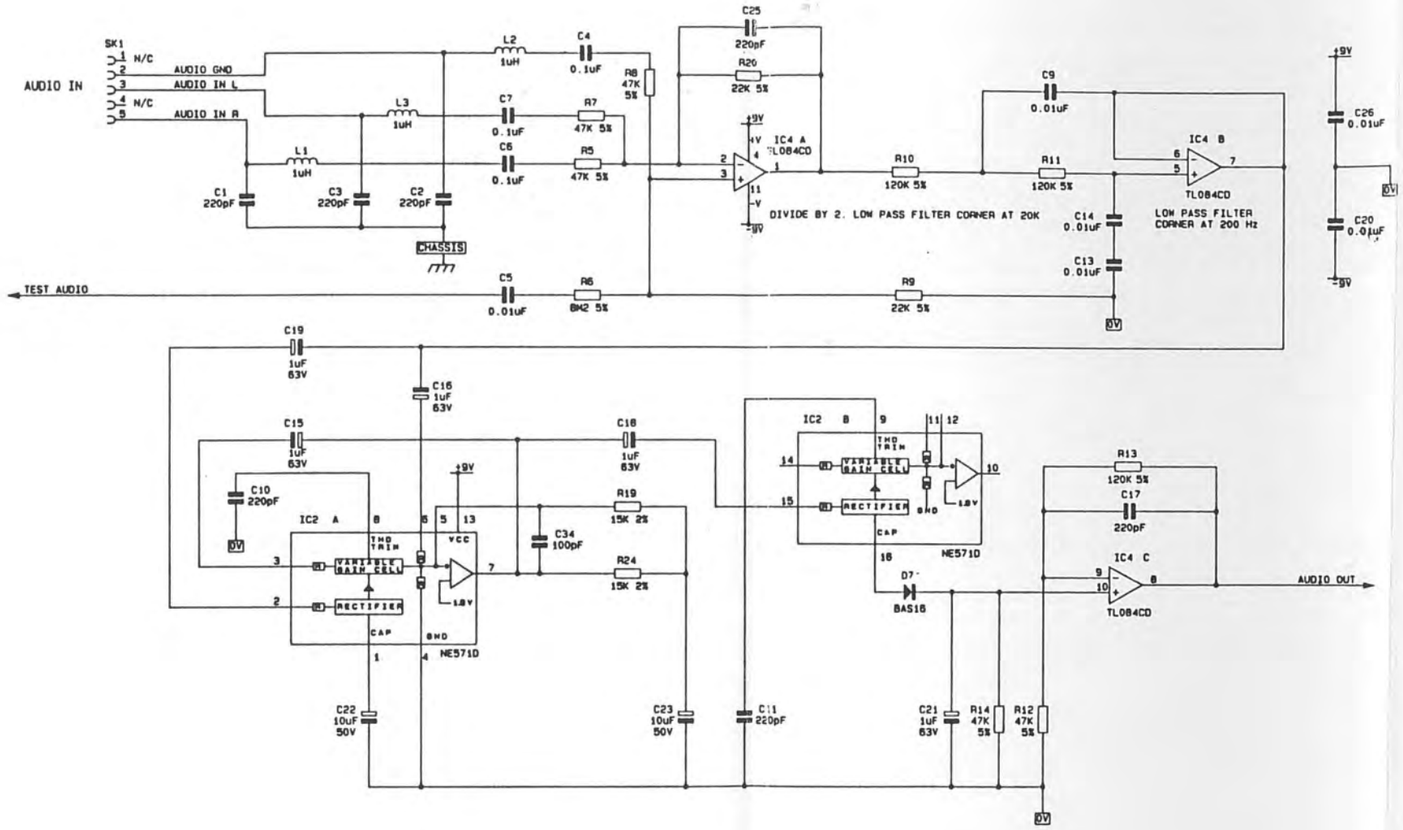
FIRST USED ON:-	DRG. No.	SH.	ISSUE
REACT IL 33227	68 40045	OF 8	1

RAPIDOS R402

DRG. No.	SH. 2	ISSUE
68 40045	OF 8	1

3RD ANGLE PROJECTION

DO NOT SCALE
IF IN DOUBT-ASK



ISSUES	
PROTOTYPE	
PRE-PROD*	
PRODUCTION	

C.No.

REV. 1.

RAPIDOS R402

I

SCALE

DIMENSIONS IN mm

TOLERANCES
1 DEC. PLACE ± 0.4 mm
2 DEC. PLACES ± 0.1 mm
ANGULAR ± 0.25°
UNLESS OTHERWISE STATED

		DATE
DRAWN	R.F	9/10/89
CHECK'D	K.C.YOUNG	6/8/90
APP'D		

Strand Lighting Ltd

Head Office: Unit 2, Cannons Business Park, Great West Isleworth, Middlesex, TW7 5QD
Tel. 01 560 3171 Telex 27978 Fax 01 568 3182
Factory: Manchester Industrial Estate, Radcliffe, Fax. 0161 3537
Tel. 0683 52333 Telex 72300 Fax. 0683 52338

MATERIAL:-

FINISH:-

FIRST USED ON:- 1L 33227
REACT

TITLE

REACT MAIN PANEL CARD.
(AUDIO INPUT).
CIRCUIT DIAGRAM.

PCB1014/1

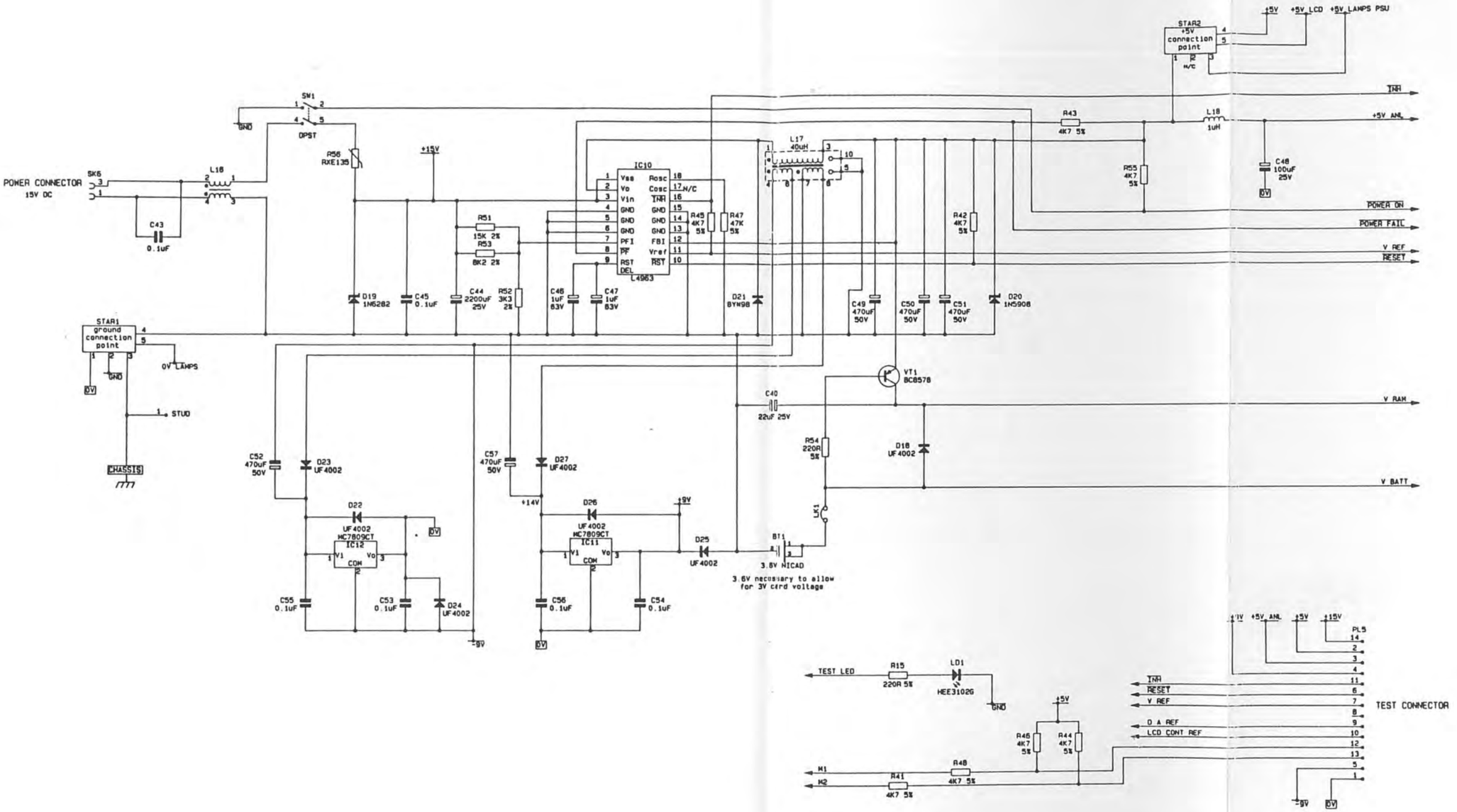
REF1952

DRG. No.	SH.2	ISSUE
68 40045	OF 8	1

DRG. No.	SH.	ISSUE
68 40045	3 OF 8	1

3RD ANGLE PROJECTION

DO NOT SCALE
IF IN DOUBT-ASK



ISSUES	
PROTOTYPE	
PRE-PROD*	
PRODUCTION	

C.No.

REV. I.

SCALE	
DIMENSIONS IN mm	
TOLERANCES 1 DEC. PLACE ± 0.4 mm 2 DEC. PLACES ± 0.1 mm ANGULAR ± 0.25° UNLESS OTHERWISE STATED	
	DATE
DRAWN R.F.	9/10/89
CHECK'D K.C.YOUNG	6/8/90
APP'D	7/8/90

I

Strand Lighting Ltd

Head Office: Unit 2, Cannons Business Park, Oram Way, Isleworth, Middlesex TW7 6QD. Tel: 01 560 3171 Telex: 27879 Fax: 01 568 2103
Factory: Manchester Industrial Estate, Rutherglen, Glasgow G73 1LT. Tel: 0698 52333 Telex: 72300 Fax: 0698 52508

MATERIAL:-	TITLE
	REACT MAIN PANEL CARD. (POWER SUPPLY) CIRCUIT DIAGRAM.
FINISH:-	PCB1014/1 REF1952
FIRST USED ON:- IL 33227 REACT	DRG. No. 68 40045 / SH.3 OF 8 / ISSUE 1

RAPIDOS R402

DRG. No.	SH. 4	ISSUE
68 40045	OF 8	1

3RD ANGLE PROJECTION | DO NOT SCALE IF IN DOUBT-ASK

+5V C24 10uF 50V R18 220R 5% GND

IC3 C 74AC14SC IC3 D 74AC14SC R4 220R 5%
IC3 A 74AC14SC IC3 B 74AC14SC R17 220R 5%
IC3 E 74AC14SC

IC1 H11L1 D2 BAS16 R3 220R 5% R2 470R 5% SK2 MIDI IN
D5 BAS16 R1 220R 5% L8 1uH SK4 MIDI THROUGH
L6 1uH D3 BAS16 CHASSIS
+9V C29 0.01uF -9V
L9 1uH D4 BAS16 CHASSIS
+5V R16 220R 5% L4 1uH SK5 MIDI OUT
D1 BAS16

IC5 SN751550 C27 220pF C28 220pF GND

L11 1uH L7 1uH
D10 FP1009 D8 FP1009 SK3 EIA-232-D I/O
R27 4K7 5% R28 4K7 5% R26 4K7 5% L5 1uH GND
R39 4K7 5% +5V CHASSIS

TXDA
ENABLE RS485 RX
ENABLE D A
RXDA
RXDB2
ENABLE RS485 TX
TXDB
RXDB1

IC9 SN7517680 L15 1uH L14 1uH R30 4R7 5% R37 220R 5% R31 4R7 5% SK3 SECONDARY SMX OUTPUT
D12 FP1009 D11 FP1009 CHASSIS

+9V C33 0.1uF C30 0.1uF -9V 0V
IC6 DAC08-ED C32 220pF -9V
OP0 OP1 OP2 OP3 OP4 OP5 OP6 OP7

RC sets the time const. of the driver to give approx. 2.5V/uS
R38 8K2 2% C38 100pF +9V C35 22uF 25V 0V
IC4 D TL084CO
IC7 LM6321N C37 22uF 25V 0V -9V
L10 1uH R40 4R7 5% PL3 D54 OUTPUT H/C 0V

D A REF
D A SET
R33 3K3 2% R23 3K3 2%
C36 10uF 50V C31 0.1uF C42 220pF
Stops processor going into TEST during RESET
RC gives less than 0.5 LSB ripple worst case
D13 BAS16 D14 BAS16 D16 BAS16 R50 4K7 5%
D A OUT
RESET
D54 SYNC
R22 3K3 2% R21 3K3 2% D6 BAS16
Also gives 0.5V noise immunity between grounds

D17 FP1009 CHASSIS R35 100R 5% PL4 AHX 192 OUTPUT
R36 100R 5% R34 100R 5%

+5V R49 4K7 5% IC8 SN7517680 L12 1uH L13 1uH D9 FP1009 CHASSIS
IC3 F 74AC14SC R32 4K7 5% GND
D15 FP1009 CHASSIS R29 4R7 5% R25 4R7 5% PL1 SMX/DMX512 OUTPUT CHASSIS

TX RS485
RX RS485

ISSUES	
PROTOTYPE	
PRE-PROD*	
PRODUCTION	

C.No.
REV. 1.

SCALE I
DIMENSIONS IN mm
TOLERANCES
1 DEC. PLACE ± 0.4 mm
2 DEC. PLACES ± 0.1 mm
ANGULAR ± 0.25°
UNLESS OTHERWISE STATED

		DATE
DRAWN	R.F.	9/10/89
CHECK'D	K.C.YOUNG	6/8/90
APP'D		

Strand Lighting Ltd
Head Office: Unit 3, Cannon Business Park, Crest Way, Isleworth, Middlesex TW7 6QD. Tel: 01 560 3171 Telex: 27978 Fax: 01 568 2153
Factory: Manchester Industrial Estate, Bakewell, Derbyshire DE45 1LT. Tel: 0629 82333 Telex: 73300 Fax: 0629 82828

MATERIAL:-
FINISH:-
FIRST USED ON:- IL 33227 REACT

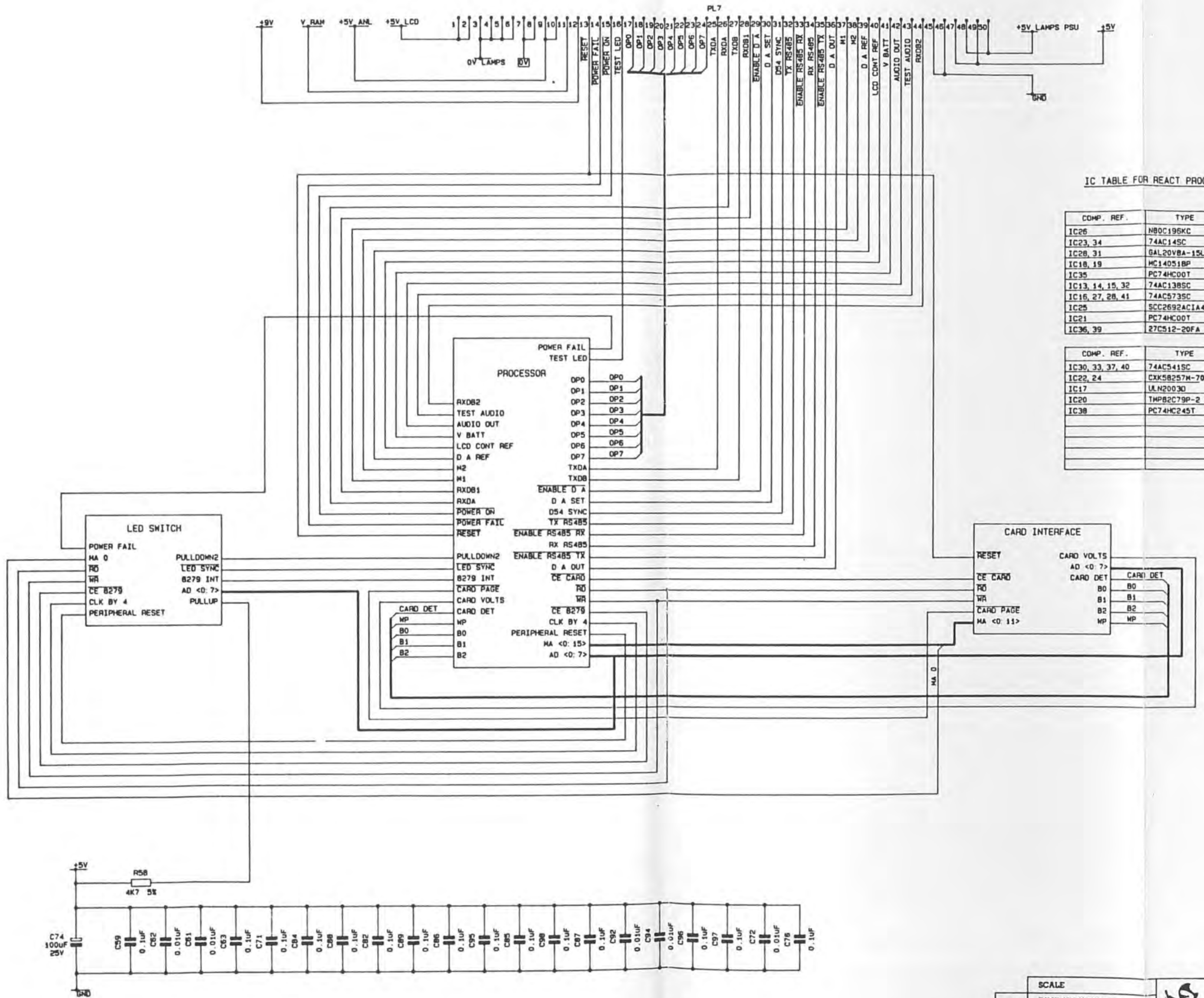
TITLE
REACT MAIN PANEL CARD. (COMMUNICATIONS). CIRCUIT DIAGRAM.
PCB1014/1 REF1952

DRG. No.	SH. 4	ISSUE
68 40045	OF 8	1

DRG. No.	SH. 5	ISSUE
68 40045	OF 8	1

3RD ANGLE PROJECTION

DO NOT SCALE
IF IN DOUBT-ASK



IC TABLE FOR REACT PROCESSOR SECTION

COMP. REF.	TYPE	Vcc	GND
IC26	N80C196KC	1	68
IC23, 34	74AC14SC	14	7
IC28, 31	GAL20V8A-15LP	24	12
IC18, 19	MC14051BP	-	-
IC35	PC74HC00T	14	7
IC13, 14, 15, 32	74AC138SC	16	8
IC16, 27, 28, 41	74AC573SC	20	10
IC25	SCC2692ACIA44	44	22
IC21	PC74HC00T	–	7
IC36, 39	27C512-20FA	30, 32	16

COMP. REF.	TYPE	Vcc	GND
IC30, 33, 37, 40	74AC541SC	20	10
IC22, 24	CXK58257M-70L	–	14
IC17	ULN2003D	–	–
IC20	TMP82C79P-2	40	20
IC38	PC74HC245T	20	10

ISSUES	
PROTOTYPE	
PRE-PROD*	
PRODUCTION	

C. No.
REV. 1.

I

SCALE
DIMENSIONS IN mm
TOLERANCES
1 DEC. PLACE ± 0.4 mm
2 DEC. PLACES ± 0.1 mm
ANGULAR ± 0.25°
UNLESS OTHERWISE STATED

		DATE
DRAWN	R.F.	12/12/89
CHECK'D	K·C·YOUNG	6/8/90
APP'D	[signature]	9/8/90

Strand Lighting Ltd

Head Office: Unit 2 Centaurs Business Park Grant Way Isleworth Middlesex TW7 5QD Tel. 01 560 3171 Telex 27976 Fax 01 568 2103
Factory: Mitchelston Industrial Estate Kirkcaldy Fife KY1 3LY Tel 0592 52333 Telex 72300 Fax 0592 53520

MATERIAL:-

FINISH:-

FIRST USED ON:- 1L 33227
REACT

TITLE
REACT MAIN PANEL CARD
(PROCESSOR SECTION BLOCK DIAGRAM)

PCB1014/1 REF1952

DRG. No.	SH.5	ISSUE
68 40045	OF 8	1

RAPIDOS R402

DRG. No.	SH. 6	ISSUE
68 40045	OF 8	1

3RD ANGLE PROJECTION

DO NOT SCALE IF IN DOUBT-ASK

IC26 — P1.0 ENABLE MIDI; P1.1 ENABLE RS485 TX; P1.2 ENABLE RS485 RX; P1.3/PWM1 LCD CONT; P1.4/PWM2 LCD LIGHT; P1.5/BREQ PERIPHERAL RESET; P1.6/RCLK PAGE SELECT; P1.7/TCLK ROM WAIT; P2.0 (TXD) TX RS485; P2.1 (RXD) RX RS485; P2.2 (EXTINT) 2692 INT; P2.3 (T2CLK) M1; P2.4 (T2RST) M2; P2.5 (PWM0) D A SET; P2.6 (T2UP-DN) ENABLE RAM; P2.7 (T2 CAP); P0.0 (ACH0) PL6 28; P0.1 (ACH1) PL6 30; P0.2 (ACH2) PL6 32; P0.3 (ACH3) PL6 34; P0.4 (ACH4) MPXR SIGNAL; P0.5 (ACH5); P0.6 (ACH6); P0.7 (ACH7) GH; VREF; AVCC; NMI; EA; RESET; VSS; VSS; VPP; AD0–AD15 AD <0: 15>; HSI.0 LED SYNC; HSI.1 8279 INT; HSI2/HSO.4 AUDIO TAIB; HSI3/HSO.5 TEST LED; HSO.0 ENABLE D A; HSO.1 D54 SYNC; HSO.2 AMX SYNC; HSO.3 TEST AUDIO; WR/WRL WR; BHE/WRH WRH; READY READY; RD RD; ALE/ADV ALE; INST INST; BUSWIDTH BUSWIDTH; CLKOUT CLKOUT; XTAL1 18MHz; XTAL2; P80C196KC

IC27 74AC573SC — AD 0–7 → MA 0–7; LE; OE PULLDOWN (R108 4K7 5%)

IC29 74AC573SC — AD 8–15 → MA 8–15; LE; OE PULLDOWN

IC36 27C512-20FA — MA 1–15 → A0–A14; ROM MA 16 → A15; PULLDOWN → A16; PGM; VPP; OE/VPP; CE; O0–O7 → AD 0–7

IC30 74AC541SC — MA 1–8 → A1–A8; DE1; DE2; Y1–Y8 → AD 0–7

IC39 27C512-20FA — MA 1–15 → A0–A14; ROM MA 16 → A15; PULLDOWN → A16; PGM; VPP; OE/VPP; CE; O0–O7 → AD 8–15

IC33 74AC541SC — MA 1–8 → A1–A8; DE1; DE2; Y1–Y8 → AD 8–15

DE ROM

IC34 A 74AC14SC — POWER FAIL → POWER FAIL; R121 470R 5%

IC35 PC74HC00T — TX RS485 → TX RS485

IC34 74AC14SC — AUDIO TAIB → AUDIO OUT; D54 → BAS16; R105 100K 5% ENABLE MIDI; VT12 BC857B; RV8 10K; R107 4K7 5%; R108 120K 5%; C100 0.01uF

R104 8K2 2%; R100 8K2 2%; C81 22pF; C83 22pF; C73 0.1uF; C91 0.1uF; R70 470R 5%; R76 4K7 5%; VT10 BC857B; C64 100uF 25V; R73 100R 5%; R96 4K7 5%; R95 4K7 5%; R97 4K7 5%; R102 4K7 5%; R98 4K7 5%; R99 4K7 5%; R91 470R 5%; MEM CORRUPT 2000H–3FFFH EXT; RESET

IC32 74AC138SC — MA 6–8 → A0–A2; E1 MA 7; E2 MA 8; E3; O0 CE 2692; O1 CE 8278; O2–O5 N/C; O6 CARD PAGE; O7 FADER PAGE; R103 4K7 5%; PULLDOWN

IC23 A 74AC14SC — PULLDOWN2

IC16 — FADER PAGE REG; AD 0–7 → MPXR A0 PL6 21; MPXR A1 PL6 22; MPXR A2 PL6 23; PL6 24; PL6 25; PL6 26; N/C 12; N/C 13

IC31 CB006101 GAL20V8A-15LP — MA 10–15 → A0–A5; ALE EXTENDED; BUSWIDTH; CLK BY 2; CLK BY 4; READY; DE ROM; ENABLE; ROM WAIT; ALE; INST; ENABLE RAM; RD; WR; CLKOUT; clkout; N/C; BUSWIDTH; CLK BY 2; CLK BY 4; READY; DE ROM

IC28 CB006001 GAL20V8A-15LP — MA 8–15 → A0–A7; RD; PAGE SELECT; WR; ENABLE RAM; INST; ENABLE PERIPHS; CE LCD; CE RAM; MEM CORRUPT; ROM MA 16; CE CARD; WRL RAM; WRH RAM

IC21 PC74HC00T — RESET; C68 0.01uF

IC21 PC74HC00T — RESET; CE RAM; R57 4K7 5%; V RAM; C78 0.1uF

IC24 CXK58257M-70L — MA 1–15 → A0–A14; VCC; WE; OE; CE; I/O0–I/O7 → AD 0–7; WRL RAM; RD

IC22 CXK58257M-70L — MA 1–15 → A0–A14; VCC; WE; OE; CE; I/O0–I/O7 → AD 8–15; WRH RAM; RD

V RAM; C77 0.1uF

SK7 — MA 0, MA 1, AD 0–AD 15, CE LCD, LCD CONT REF

IC18 MC14051BD — MPXR A0–A2; BATT VOLTS; CAL VOLTS; CARD VOLTS; D A REF; D A OUT; LCD CONT REF; TIME A; TIME B; MPXR SIGNAL; R80 100K 5%; V BATT; C66 0.01uF; R81 470R 5%

IC19 MC14051BD — MPXR A0–A2; MPXR SELECT; RV3–RV11 10K; C67 0.01uF; MPXR SIGNAL; TIME B; TIME A; GH; RV2 10K GRAND MASTER; RV1 10K; RV12 10K; C101 0.1uF; C90 0.1uF; C75 0.1uF; C60 0.1uF

SCC2692ACIA44 IC25 — MA 0–3; CARD DET; WP; CLK BY 2; POWER ON; B0; B1; B2; RXDA; RXDB; CE 2692; WR; RD; PERIPHERAL RESET; AD 0–7; IP0–IP6; OP0–OP7; CEN; WRN; RDN; RESET; TXDA; TXDB; INTRN; X1/CLK; X2; R101 100K 5%; XTAL2 3.6864MHz; C79 22pF; C80 22pF; R94 4K7 5%; IC23 C 74AC14SC — 2692 INT

+5V LCD; L20 1uH; C69 100uF 25V; C70 0.1uF; 0V LAMPS; VT11 BST60; R88 4K7 5%; LCD LIGHT; R90 1R0 5%; R92 1R0 5%; R93 1R0 5%; +5V ANL; +9V; +5V LAMPS; PL6; SK8 CKLIGHT

IC23 D 74AC14SC — RXDB; IC35 PC74HC00T; IC23 E 74AC14SC; IC21 PC74HC00T; R89 4K7 5%; IC21 PC74HC00T; IC23 F 74AC14SC — RXDB1; ENABLE RS485 RX

RXDB2 — Takes data from either EIA-232-D or RS 485 receiver

NOTE: PIN OUTS FOR 27C512-20FA (IC36, 39) ARE DISPLACED BY 2 BECAUSE A 28 PIN DEVICE IS FITTED IN A 32 PIN SITE, THIS DEVICE THEREFORE OCCUPIES PINS 3–30.

ISSUES	
PROTOTYPE	
PRE-PROD*	
PRODUCTION	

C.No. REV. I.

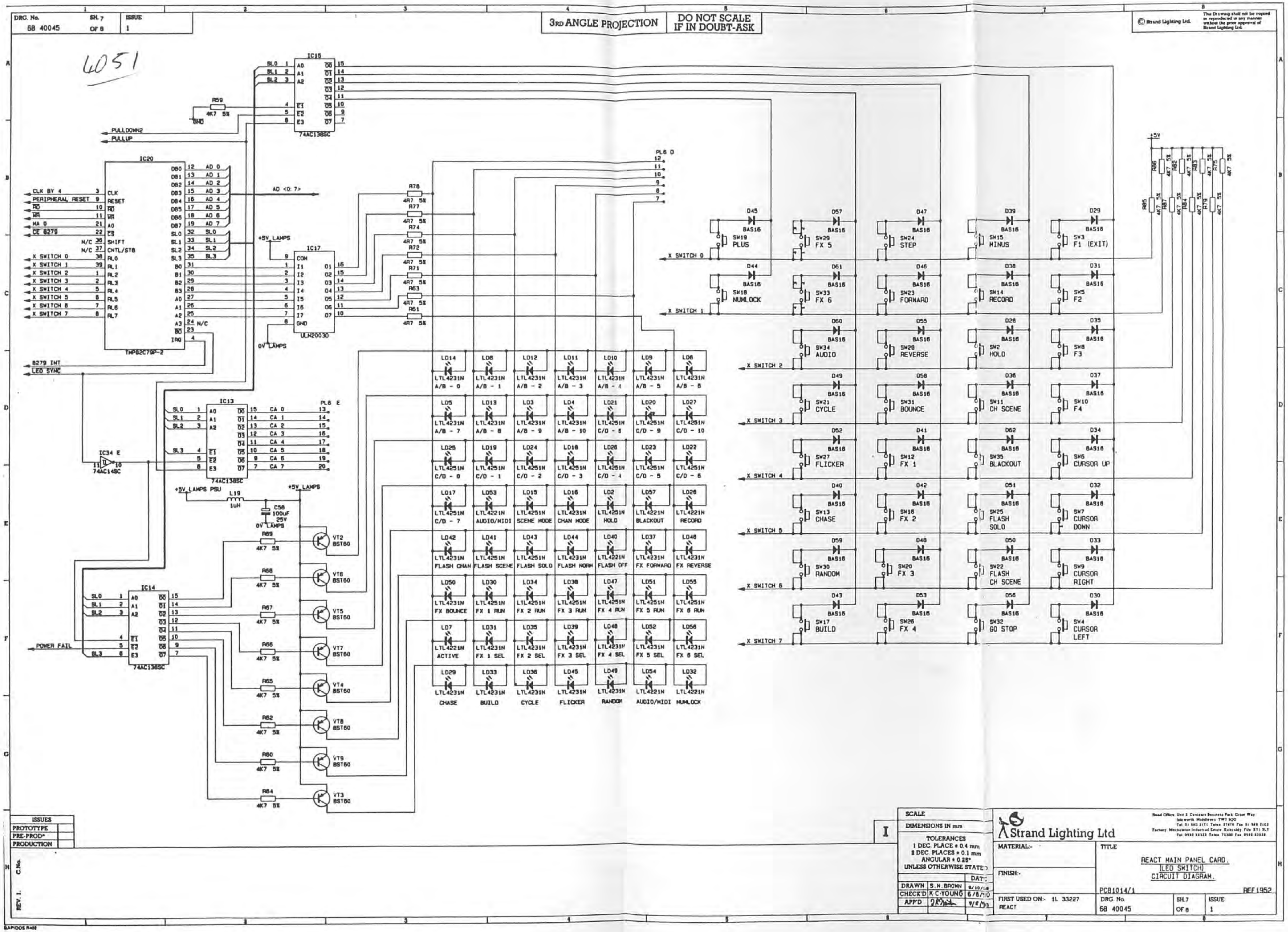
SCALE		I
DIMENSIONS IN mm		
TOLERANCES 1 DEC. PLACE ± 0.4 mm; 2 DEC. PLACES ± 0.1 mm; ANGULAR ± 0.25° UNLESS OTHERWISE STATED		
	DATE	
DRAWN S.N.Brown	5/10/89	
CHECK'D K.C.YOUNG	6/8/90	
APP'D	9/8/90	

Strand Lighting Ltd

Head Office: Unit 3, Cremorne Business Park, Great Way, Isleworth, Middlesex TW7 5QD. Tel. 01 560 3171 Telex 27879 Fax 01 568 2102. Factory: Manchester Industrial Estate, Rochdale, Lancs. OL11 2LT. Tel. 0592 51333 Telex 73308 Fax 0592 53539

MATERIAL:-	TITLE: REACT MAIN PANEL CARD (PROCCESSOR) CIRCUIT DIAGRAM
FINISH:-	PCB1014/1 — REF1952
FIRST USED ON:- IL 33227 REACT	DRG. No. 68 40045 — SH. 6 OF 8 — ISSUE 1

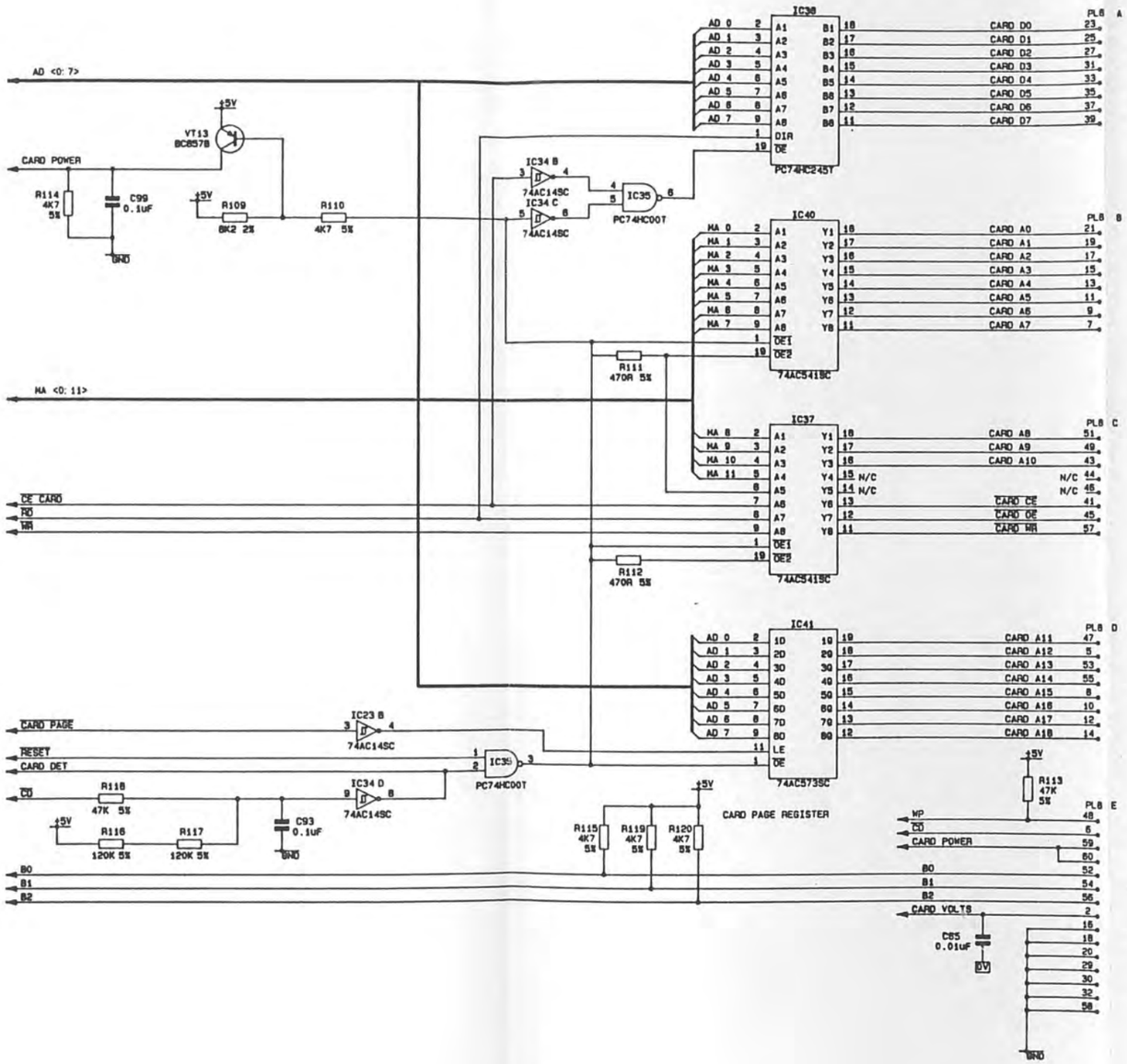
RAPIDOS R402


DRG. No. 68 40045
SH. 7 OF 8
ISSUE 1
3RD ANGLE PROJECTION
DO NOT SCALE IF IN DOUBT-ASK
4051
IC15
74AC138SC
IC20
TMP82C79P-2
IC17
ULN2003D
IC13
74AC138SC
IC14
74AC138SC
IC34 E
74AC14SC
PULLDOWN2
PULLUP
CLK BY 4
PERIPHERAL RESET
X SWITCH 0
X SWITCH 1
X SWITCH 2
X SWITCH 3
X SWITCH 4
X SWITCH 5
X SWITCH 6
X SWITCH 7
8279 INT
LED SYNC
POWER FAIL
AD <0: 7>
+5V LAMPS
0V LAMPS
+5V LAMPS PSU
PL6 D
PL6 E
SW19 PLUS
SW29 FX 5
SW24 STEP
SW15 MINUS
SW3 F1 (EXIT)
SW18 NUMLOCK
SW33 FX 6
SW23 FORWARD
SW14 RECORD
SW5 F2
SW34 AUDIO
SW28 REVERSE
SW2 HOLD
SW8 F3
SW21 CYCLE
SW31 BOUNCE
SW11 CH SCENE
SW10 F4
SW27 FLICKER
SW12 FX 1
SW35 BLACKOUT
SW6 CURSOR UP
SW13 CHASE
SW16 FX 2
SW25 FLASH SOLO
SW7 CURSOR DOWN
SW30 RANDOM
SW20 FX 3
SW22 FLASH CH SCENE
SW9 CURSOR RIGHT
SW17 BUILD
SW26 FX 4
SW32 GO STOP
SW4 CURSOR LEFT
ISSUES
PROTOTYPE
PRE-PROD*
PRODUCTION
SCALE
DIMENSIONS IN mm
TOLERANCES
1 DEC. PLACE ± 0.4 mm
2 DEC. PLACES ± 0.1 mm
ANGULAR ± 0.25°
UNLESS OTHERWISE STATED
DRAWN S.N.BROWN
CHECK'D K.C.YOUNG 6/8/90
Strand Lighting Ltd
MATERIAL:-
FINISH:-
FIRST USED ON:- 1L 33227 REACT
TITLE
REACT MAIN PANEL CARD.
(LED SWITCH)
CIRCUIT DIAGRAM.
PCB1014/1
REF 1952
DRG. No. 68 40045
SH.7 OF 8
ISSUE 1

DRG. No.	SH. 8 OF 8	ISSUE 1

3RD ANGLE PROJECTION | DO NOT SCALE IF IN DOUBT-ASK

CARD CONNECTOR



ISSUES	
PROTOTYPE	
PRE-PROD*	
PRODUCTION	

C.No.

REV. 1.

I

SCALE

DIMENSIONS IN mm

TOLERANCES
1 DEC. PLACE ± 0.4 mm
2 DEC. PLACES ± 0.1 mm
ANGULAR ± 0.25°
UNLESS OTHERWISE STATED

		DATE
DRAWN	R.F.	8/11/89
CHECK'D	K C YOUNG	6/8/90
APP'D		7/9/90

Strand Lighting Ltd

Head Office, Unit 3, Centaurs Business Park, Grant Way, Isleworth, Middlesex TW7 5QD
Tel. 01 560 3171 Telex 27976 Fax. 01 568 2103
Factory: Manchester Industrial Estate, Eccleshill, Pde. BD1 3LY
Tel. 0532 52333 Telex. 72300 Fax. 0532 52316

MATERIAL:-

FINISH:-

TITLE

REACT MAIN PANEL CARD
(CARD INTERFACE)
CIRCUIT DIAGRAM

PCB1014/1 REF.1952

FIRST USED ON:- 1L 33227
REACT

DRG. No.	SH.8	ISSUE
68 40045	OF 8	1

RAPIDOS R402

DRG. No. 6840046 SH. 1 OF 1

3rd ANGLE PROJECTION

DO NOT SCALE IF IN DOUBT ASK

COMP. REF.	TYPE	Vcc +5V ANL	GND 0V ANL
IC1	CA5160E	-	4
IC2-9	MC14501BCP	16	8

NOTES:
a.) ANALOGUE 0V NOTATED VIA :- 0V
b.) ALL RESISTORS ARE SFR25 0.4W UNLESS STATED.

SCHEDULE : 5533221
DRILLING : 5840173

PROTOTYPE USE			
PRE-PROOFS USE			
PRODUCTION USE			
ISSUE	C.No.		

Strand Lighting Ltd

Head Office: Great Way (off Syon Lane) Isleworth, Middlesex, TW7 5QD. Tel: 081-568-2111. Telex: 27674. Fax: 081-568-2105. Factory: Manchester Industrial Estate, Edmondsley, Co. Durham, DH7 6LT. Tel: 0385-63333. Telex: 71300. Fax: 0385-63005.

MATERIAL:-

FINISH:-

FIRST USED ON:- 1L33227 REACT

DIMENSIONS IN mm
TOLERANCES
1 DEC. PLACE ± 0.4mm
2 DEC. PLACES ± 0.1mm
ANGULAR ± 0.25°
UNLESS OTHERWISE STATED

SCALE		DATE
DRAWN	B.N. BROWN	05.11.90
CHECK'D	R.C. YOUNG	21.11.90
APP'D	A.R.B	22.11.90

TITLE
REACT FADER WING
CIRCUIT DIAGRAM

PCB1015/2 REF1953

ISSUE 1

DRG. No. 6840046

SH. 1 OF 1