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Designer's Control

USER'S HANDBOOK

88-020-10
40/B206

Strand Lighting

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CHAPTER 1

INTRODUCTION

1.1 GENERAL

The Designer's Control is a hand held unit which allows remote control of Rank Strand memory lighting control systems. The unit plugs into a Rigger's Bus, connected to the host system, which has outlets positioned conveniently around the lighting galleries. Users who require a system which gives complete freedom of movement may connect the Designer's Control Infra-red Receiver to the Rigger's Bus. The infra-red signal transmitted by the Designer's Control is not visible to the eye. Note that the wired and infra-red systems cannot be used simultaneously on the same installation.

The Designer's Control provides comprehensive operational facilities, allowing complete control of individual and groups of channels, the recording of lighting states in the host system memory and the recall of memories, both as instant and fade actions.

Power for the unit is provided by internal rechargeable batteries, and power saving circuitry is incorporated which ensures adequate battery life between charges.

A single Rank Strand Rigger's Control may be used at the same time as the Designer's Control on systems using a Rigger's Bus. In the case of the Infra-red system, only a single Designer's Control may be used.

1.2 TECHNICAL SPECIFICATION

1.2.1 Designer's Control

Supply	5 x AA size quick charge nickel-cadmium cells (7.5V, 500mAH).

CHAPTER 2

INSTALLATION

2.1 DESIGNER'S CONTROL

2.1.1 Unpacking

The Designer's Control is supplied packed in a cardboard carton with foam protection. Unpack it carefully to avoid damage and retain the packing in case the unit needs to be returned for repair. Check that the following items are enclosed:

1 Designer's Control unit.
1 Battery charger.
1 13 amp socket.
1 Connecting lead.
1 User's Handbook.
1 6-way Hypertac plug.

The Infra-red receiver unit is supplied separately.

2.1.2 Connections

The Designer's Control connects to the Rigger's Bus by means of the lead supplied, which is terminated at each end in a 5-way Cannon XLR connector. The Rigger's Bus connects to the host system via a 6-way Smith Hypertac connector. The wiring of these connectors is given in Table 2.1.2.

2.2 INFRA-RED RECEIVER

2.2.1 Connections

The Infra-red Receiver, when provided, requires a mains input (240 or 120 volts) and connects to the Rigger's Bus by means of a flying lead terminated in a 5-way Cannon XLR connector. No connections to

Table 2.1.2

Signal	XLR	Hypertac
R+	Pin 1	Pin 1
R-	Pin 2	Pin 2
Radio On	Pin 4	
Radio Data	Pin 5	
Ground	Pin 3	Pin 6

the Designer's Control are necessary as the Infra-red transmitter is an integral part of the unit.

2.2.2 Installation

The Infra-red Receiver incorporates an adjustable suspension bracket, fitted with an M10 bolt, which may be attached to any of the standard lantern fixings (hook clamps, wall brackets, etc.). Always use a safety bond to supplement the main suspension (a safety bond strap is provided on the body of the unit).

The unit should be positioned so as to cover as much of the working area as possible, bearing in mind the 30 metre line-of-sight range and the acceptance angle (see section 1.2.2). If the whole area cannot be covered, additional receiver units should be used. When positioning, ensure that no light shines directly into the horn and that the unit is well away from any fluorescent fittings.

CHAPTER 3

OPERATION

3.1 PRELIMINARY

As a preliminary to any lighting exercise, check that the host system and its dimmers are operating and that the Designer's (or Rigger's) Control input is enabled. If the system is fitted with an Infra-red receiver, ensure that the latter is connected to the mains supply and that its power-on indicator is illuminated.

Connect the Designer's Control to the Rigger's Bus, if provided, and turn the unit On by moving the switch marked 'O-1' to the '1' position. Assuming that the batteries are charged sufficiently, the LED indicator above the switch will light.

Note: The following describes the operational facilities provided on the Designer's Control. How these function in practice depends on the type of host system. There are, for instance, detail differences between operation with Galaxy and operation with Lightboard. If in doubt, experiment.

3.1.1 Battery Charging

Before using the Designer's Control, ensure that its internal batteries have sufficient charge. If the charge is low, the brightness of the displays and indicators will be noticably reduced.

The charger connects to the Designer's Control via a 2.5mm jack plug and incorporates an integral 13A plug for connection to the mains. A mating socket is also supplied so that an adaptor lead may be constructed for locations where 13A outlets are not available.

The unit will require charging after about four hours of normal operation and will take about five hours to become fully recharged. Do not leave the unit charging for longer than ten hours. Note also that the unit may be operated normally while on charge.

3.1.2 Power Saving Mode

In order to increase the period for which the Designer's Control may be used before recharging becomes necessary, the display and the LEDs (except the Power On LED) will be automatically extinguished after about 30 seconds if no operations are carried out. The displays will be restored when any key is operated, although they may also modified by the key action concerned. To restore the displays without any modification, press C (Clear).

3.2 CHANNEL AND MEMORY NUMBERS

Because there is no provision for the transmission of data from the host system to the Designer's Control, it is important that the operator know which channels and memories are available for use. All channel numbers from 1 to 999 and memory numbers from 0.1 to 999.9 may be selected, but no warning can be given that a channel or memory number is invalid. Operations involving invalid channel or memory numbers will simply have no effect. More important, no warning is given on over-recording an existing memory, so that the operator must know which valid memory numbers must not be used.

3.3 CHANNEL CONTROL MODE

In its normal mode of operation, the Designer's Control is used for the selection of lighting channels and for setting and adjusting their levels. Channel numbers are selected on the keypad and appear on the left-hand (CHAN/MEM) side of the display window.

3.3.1 Setting Channel Levels

Following selection of a channel number, its level may be set by either of the following methods:

i) By operation of the '@' key, followed by a single digit, or by two digits separated by a decimal point ('.'). These digits represent levels on a scale of ten and may be considered as a percentage. Thus 5 will set the selected channel to 50% and

5.5 to 55%. The key marked F selects maximum level (1ØØ%). The resulting channel level is shown as a percentage on the right-hand (LEVEL) side of the display window.

When the '@' key is pressed, the adjacent LED indicator lights to warn that the next entry will be interpreted as a level. Once the first level digit has been entered, the LED is extinguished, but it will light again if the '.' key is operated, to indicate that the least significant digit of the level may be entered.

ii) By use of the '∧' (Up) and '∨' (Down) keys. When either is held down the selected channel fades up or down, as appropriate, at a fixed rate, taking approximately seven seconds to fade from zero to full. If a channel is faded up from zero using the '∧' key its level will be prefixed '+' in display window.

When a channel level has been set (by either of the above methods) the keypad becomes immediately available for a new selection. There is no need to operate the Clear (C) key before selecting the next channel.

3.3.2 Modifying Channel Levels

The level of any channel which is already contributing to the lighting may be easily adjusted by selecting the channel required and then using the '@' key or the '∧' or '∨' keys. If the latter keys are used, the display window cannot show the absolute level of the channel, but will display the percentage change, preceded by '+' or '-' as appropriate.

If required, the '@' key may be used in conjunction with the '+' and '-' keys to adjust the level by a predetermined amount. For example, to raise channel 8 by 1Ø% press 8, '@', '+', 1. Use of the decimal point as previously described allows modification to 1% accuracy.

3.3.3 Selection and Control of Groups of Channels

The ability to control the level of several channels simultaneously (i.e. as a group) is highly desirable and speeds up rehearsals considerably. The channels constituting a group may be selected individually by the following procedure:

i) Enter first channel, e.g. 26.
ii) Enter '+'.
iii) Enter second channel, e.g. 183.
iv) Enter '+'.
v) Enter third channel, e.g. 114.
Etc. ...

Channels 26, 114 and 183 would then be controlled together as one channel.

Similarly, a channel may be removed from control as follows:

i) Enter '-'.
ii) Enter channel, e.g. 114.

The display window always shows the number of the last channel selected.

If all the channels selected are at the same level when taken under control they remain together when the Up (∧) or Down (∨) keys are operated. If, however, the channels are at different levels, an equal amount is added to or subtracted from each channel as they fade up or down. This type of fade is not proportional and is usually referred to as a 'Group' or 'Shaft' fade.

The Up (∧) key may be pressed and held down until one-by-one all channels reach full. Operating the Down (∨) key will then restore the original balance, while further downward movement reduces the levels until one-by-one the channels reach zero.

3.3.4 Incremental Channel Selection

The '+1' and '-1' keys select respectively the next or the preceding channel number. When adjusting a sequence of channels, use of these keys avoids the need to select the individual channel number digits.

3.3.5 Use of the ON Key

The On facility provides a convenient method of rapidly setting channels to a preferred level. With a valid channel selection, pressing the ON key turns the channel or channels On, while a second operation turns the channels Off. The ON key will operate on individual channels or groups.

The level to which channels are set is always 70%, unless the operator has changed the level as follows:

i) Select a channel or group of channels.
ii) Press 'ON' (The channels will now be set to 70%).
iii) Use the '@' key to set the channels to the preferred level (note that the '∧' and '∨' keys may not be used to set the ON level).
iv) Press ON again. (The channels will be turned off).

The revised level will then be used as the preferred level for any subsequent operation of the ON key.

3.4 RECORDING LIGHTING STATES

3.4.1 Selecting Record Mode

Once a lighting state has been set-up to the operator's satisfaction, it may be recorded in the memory on the host system. First ensure that recording is enabled on the main desk (some systems may have a separate 'Designer's Record' keyswitch) and then press the REC key above the display window. The adjacent LED lights, and the display window and the other LEDs clear, allowing the required memory number to be entered on the keypad.

3.4.2 Memory Selection

Any integer between 1 and 999 may be selected on the keypad and, in addition, nine memory numbers, identified by a digit following a decimal point, between each integer, e.g. 32.1, 32.2, 32.3, etc. Normally, when recording, integer numbers would be used first (1, 2, 3, etc.) and then, if it became necessary to insert a state between, say, memories 2 and 3, memory 2.5 could be used.

Note that the memories available are determined by the host system and it is important to know the permitted range (and whether numbers between integers are available) as there is no warning given, either of attempting to use a non-existent memory or of over-recording.

3.4.3 Performing the Record Action

The record action takes place when the REC key is operated a second time. Designer's Control record actions are the equivalent of Record System Output on the main desk and all lighting will be recorded, whether set-up using the Designer's Control or the host system control panels.

When the REC key is pressed the second time, the adjacent LED is extinguished and the display and LEDs return to the state which was current at the start of the record action.

3.5 RECALLING MEMORIES

Memories may be recalled in three ways, selected by the '↕' (Group), '↑↓' (Move-fade) and '✕' (Crossfade) keys above the keypad.

3.5.1 Group

When a memory is recalled as a Group, the effect is the same as using the '+' key to select all the channels which are ON in the memory. The channels may then be faded up or down together as a 'Group' or 'Shaft fade using the '∧' and '∨' keys (see section 3.3.3), the recorded channel levels being ignored.

To recall a memory as a Group, press the '↕' key (the adjacent LED lights) and then select the number of the memory required. If required, individual channels and Group memories may be combined for control using the '+' and '-' keys. For example, to add a memorised group to the channels already under control, enter '+', '↕' followed by the memory number.

When controlling a group of channels, pressing the '@' key followed by a number sets all channels under control to the chosen level. However, prefixing the number with '+' or '-' will cause each channel to be increased or decreased by the same amount (within the limits of full and zero), thus preserving the differences.

3.5.2 Control of Move-fades or Crossfades

In addition to controlling previously recorded memories as groups (see section 3.5.1), the Designer's Control may be used to recall memories with the associated channels at their recorded levels and to carry out Move-fades. When the Designer's Control is used in this way, channels 'On' in a selected memory will proportionally fade to their recorded levels when the '∧' key is operated. In this way a scene may be lit by combining several memories which have been balanced separately. A Move-fade does not affect channels which are not On in the selected memory.

Move-fade mode is selected by pressing the Move (↑↓) key before entering the required memory number. The adjacent LED lights to indicate that Move-fade mode is selected.

Two or more memories may be combined for introduction simultaneously by using the following procedure:

i) Press the Move (↑↓) key.
ii) Select the first memory on the keypad.
iii) Press the '+' key.
iv) Press the Move key.
v) Select the second memory.
vi) Continue until the required combination is obtained.

Note that if additional channels or groups are added to a combination prepared as above, the whole selection becomes a group and the fade changes from a Move-fade to a 'Group' or 'Shaft' fade. This is because there are no recorded destinations for the additional channels.

If a Move-fade is prefixed with '-' the channels that are On in the selected memory will dim out when the '∧' key is operated.

Finally, the Designer's Control is able to carry out complete Crossfades to memorised lighting states. That is, the current lighting is substituted entirely by the lighting set in a recorded memory, channels that are Off in the memory fading out. The procedure for this is to simply prefix the required memory number with Crossfade (X). As in the case of a Move-fade action, memories may be combined before starting a Crossfade.

Note that when the '@' key is used in conjunction with a Move-fade or Crossfade (which are proportional fades) the 'level' entered is taken as the percentage of that fade carried out and channels are set immediately to the levels which they would achieve by fading. For example, 'X', 10, '@', 5 would switch all channels from their current levels to the levels they would achieve half way (50%) through a crossfade to memory 10.

3.6 VDU PAGE CONTROL

Where the host system has more channels in use than can be displayed on one screen of the mimic display, the key labelled 'PG' (Page) may be used to step to the second and subsequent pages of the VDU display.

CHAPTER 4

TECHNICAL DESCRIPTION

4.1 GENERAL

The Designer's Control and Infra-red Receiver contain few user-replacable parts. REPAIRS SHOULD ONLY BE CARRIED OUT BY QUALIFIED ENGINEERS AUTHORISED TO MAINTAIN THIS EQUIPMENT.

4.1.1 Conventions

When using this section of the handbook, the following conventions should be noted:

i) Whenever numbers are used, they are decimal (i.e. to base 10) unless prefixed with a dollar ($) sign, in which case the number is hexadecimal (base 16).

ii) Integrated circuits are identified by their component number, prefixed with the letters IC (e.g. IC7). Where an integrated circuit contains more than one logic element, the output pin number of the element concerned is added as a suffix, e.g. IC13/4. In the case of elements with two or more outputs, e.g. bistables, one of the outputs is chosen for identification purposes, depending on the context.

iii) The term 'pin' is used to identify connections to integrated circuits. Connections to printed circuit boards are referred to as 'board terminal' or simply 'terminal'.

iv) Logic levels depend on whether the logic concerned is TTL or CMOS. In the case of TTL, >2.4V equals logic 1 and <0.8V logic 0, while CMOS levels are >3.5V for logic 1 and <1.5V for logic 0, unless the rails to the device concerned determine otherwise. Where a signal is low active, this is indicated in the text and on the circuit diagrams.

4.1.2 Glossary of Terms

The following lists abbreviations and mnemonics used in the technical description:

A0 to A12	Address Bus lines (13 bits) - A0 is the least significant bit. A0 - A7 are multiplexed on the Data/Address bus (B0 - B7) and are valid on the trailing edge of 'AS'
AS	Address Strobe - See above (A0 - A12).
D0 to D7	Data Bus lines (8 bits) - Data is valid on the trailing edge of 'DS'. D0 is the least significant bit. These lines also carry multiplexed address information which is valid on the trailing edge of 'AS'.
DS	Data Strobe - See above (D0 - D7).
EPROM	Erasable Programmable Read-only Memory.
IRQ	Interrupt Request.
PROM	Programmable Read only Memory.
R/W	Read or Write - This signal indicates the direction of data transfer on the Data Bus (with respect to the MPU) and is low for Write. It is valid on the rising edge of 'DS'.
RESET/RST	Reset Signal - The RESET line is held low during the initial power-on sequence to ensure correct initialisation.
RAM	Random Access Memory.

4.2 TRANSMISSION FORMAT

The Designer's Control produces three output signals: Rigger's Bus, Infra-red and Radio. These are all asynchronous serial signals at 2400 baud, but each has a different form as described in sections 4.2.2, 4.2.3 and 4.2.4.

4.2.1 Data Format

All transmissions consist of a data frame of four bytes of data. Each byte comprises a start bit ('0'), eight data bits, a parity bit (odd parity) and a stop bit ('1'). The function of each byte is as follows:

	Bit 7		Bit 0
Byte 1	T1		T2
Byte 2	T3		T4
Byte 3	Action Code	Use Code	Function Code
Byte 4	Level		

The type of action to be performed is determined by the Function Code (see Table 4.2.1.1) and the latter also determines how T1 - T4 are interpreted by the host system (see below). Note that the Rigger's Control transmits in a similar format (using three bytes instead of four) and that the relevant codes are included here for completeness.

	T1	T2	T3	T4
Rigger's Channel No.	1000s	100s	10s	1s
Designer's Channel No.	100s	10s	1s	.1s
Memory No.	100s	10s	1s	.1s

Note: In the case of the Rigger's Control channel number, T1 (1000s) is not normally used.

Table 4.2.1.1

Action Code	Use Code	T1 - T4
Function Code equals 0 - Channel Control (Rigger's)		
0 - Fade Down (⋁) 1 - Set Zero (⩛) 2 - Fade Up (⋀) 3 - Set On (⩓)	0 - 3 (Note 1) " " " " " "	Rigger's Channel No. " " " " " " " " "
Function Code equals 1 - Channel Control		
0 - Set Level 1 - Add Level 2 - Subtract Level 3 - Not Used	0 - Take Channel 1 - Add Channel 2 - Subtract Channel 3 - Use Existing Chan.	Designer's Chan. No. " " " " " " " " "
Function Code equals 2 - Pan, Tilt and Focus		
0 - Set Level 1 - Add Level 2 - Subtract Level 3 - Not Used	0 - Pan 1 - Tilt 2 - Focus 1 3 - Focus 2	Designer's Chan. No. " " " " " " " " "
Function Code equals 3 - Iris Control		
0 - Set Level 1 - Add Level 2 - Subtract Level 3 - Not Used	0 - Iris 1 - Not Used 2 - Not Used 3 - Not Used	Designer's Chan. No. " " " " " " " " "
Function Code equals 4 - Hoist Control		
0 - Set Level 1 - Add Level 2 - Subtract Level 3 - Not Used	0 - Not Used 1 - Hoist X Axis 2 - Hoist Y Axis 3 - Not Used	Designer's Chan. No. " " " " " " " " "
Function Code equals 5 - Not Used		
Function Code equals 6 - Barn Door/Shutter Position		
0 - Set Level 1 - Add Level 2 - Subtract Level 3 - Not Used	0 - Barn Door/Shutter 1 1 - Barn Door/Shutter 2 2 - Barn Door/Shutter 3 3 - Barn Door/Shutter 4	Designer's Chan. No. " " " " " " " " "

Table 4.2.1.1 (cont.)

Action Code	Use Code	T1 - T4
Function Code equals 7 - Barn Door/Shutter Rotation		
0 - Set Level 1 - Add Level 2 - Subtract Level 3 - Not Used	0 - Rotate 1 - Not Used 2 - Not Used 3 - Not Used	Designer's Chan. No. " " " " " " " " "
Function Code equals 8 - Colour Change Control		
0 - Set Colour 1 - Add Colour 2 - Subtract Colour 3 - Not Used	0 - Take C/C 1 - Add C/C 2 - Subtract C/C 3 - Use Existing C/C	Designer's Chan. No. " " " " " " " " "
Function Code equals 9 - Memory Control (Rigger's)		
0 - Dim (∨) 1 - Wipe (⩒) 2 - Move (∧) 3 - Cut (⩓)	0 - 3 (Note 1) " " " " " "	Memory Number " " " " " "
Function Code equals $A (10) - Memory Move-fade		
0 - Set Level 1 - Add Level 2 - Subtract Level 3 - Not Used	0 - Take Memory 1 - Add Memory 2 - Dim Memory 3 - Use Existing Mem.	Memory Number " " " " " "
Function Code equals $B (11) - Memory Crossfade		
0 - Set Level 1 - Add Level 2 - Subtract Level 3 - Not Used	0 - Take Memory 1 - Add Memory 2 - Dim Memory 3 - Use Existing Mem.	Memory Number " " " " " "
Function Code equals $C (12) - Memory Group Control		
0 - Set Level 1 - Add Level 2 - Subtract Level 3 - Not Used	0 - Take Memory 1 - Add Memory 2 - Dim Memory 3 - Use Existing Mem.	Memory Number " " " " " "
Function Code equals $D (13) - Not Used		
Function Code equals $E (14) - Not Used		

Table 4.2.1.1 (cont.)

Action Code	Use Code	T1 - T4
Function Code equals $F (15) - Record/System Commands		
Ø - Record Action 1 - Not Used	Ø - Record Lighting 1 - Record C/C 2 - Record Position 3 - Not Used	Memory Number " " " " " "
2 - System Command 3 - Not Used	Ø - Page VDU 1 - Not Used 2 - Not Used 3 - Not Used	- - - -

Notes: 1) Identifies a particular Rigger's Control unit (1 of 4).

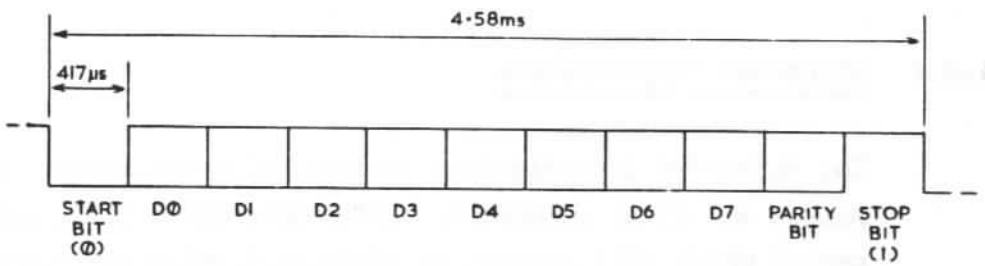
2) Function Codes Ø and 9 are used only by the Rigger's Control.

3) Function Codes 2, 3 and 8 are used only on Designer's Control units configured for limited PTF.

4) Function Codes 4, 6 and 7 are used only on Designer's Control units configured for full PTF.

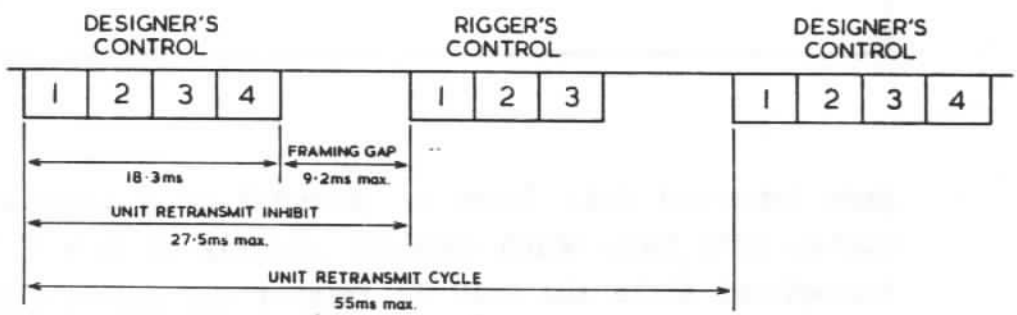
4.2.2 Rigger's Bus Transmissions

Each byte transmitted on the Rigger's Bus takes the form shown in Fig. 4.2.2.1.



RIGGERS BUS DATA
FIG. 4.2.2.1

The four bytes forming a data frame are transmitted sequentially, followed by a gap of 9.2ms, i.e. long enough for a time-out circuit in the host system to detect with certainty that transmission has ceased. Because of this, the unit must wait until the bus has been free for this period before starting a transmission.

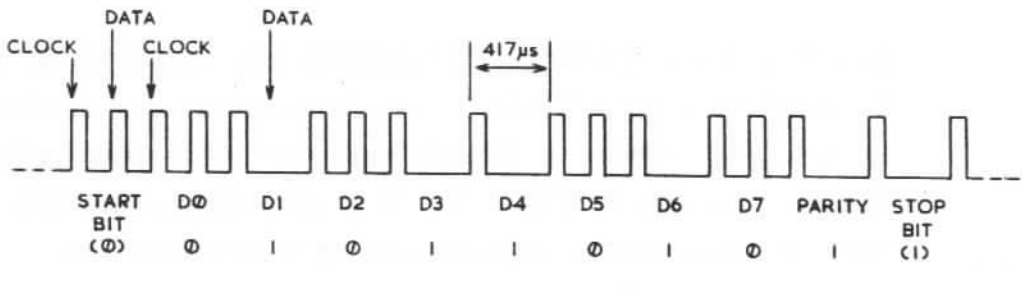


DATA FRAME TIMING
FIG. 4.2.2.2

When the Designer's Control is fading channels or memories, it must transmit continuously to ensure a smooth fade action. In practice, this means that only one Rigger's Control can use the Rigger's Bus at the same time as the Designer's Control. To allow a second unit to transmit, the Designer's Control will wait 27.5ms between data frames when transmitting continuously. Fig. 4.2.2.2 shows the bus timing when two units are using the bus.

4.2.3 Infra-red Transmissions

The Infra-red transmissions consist of a continuous stream of clock pulses at 417us intervals. Following each clock pulse is a data period which will contain an additional pulse to represent a '0'. If there is no additional pulse the data is '1'. The format of a byte of data is shown in Fig. 4.2.3.1.



INFRA-RED DATA

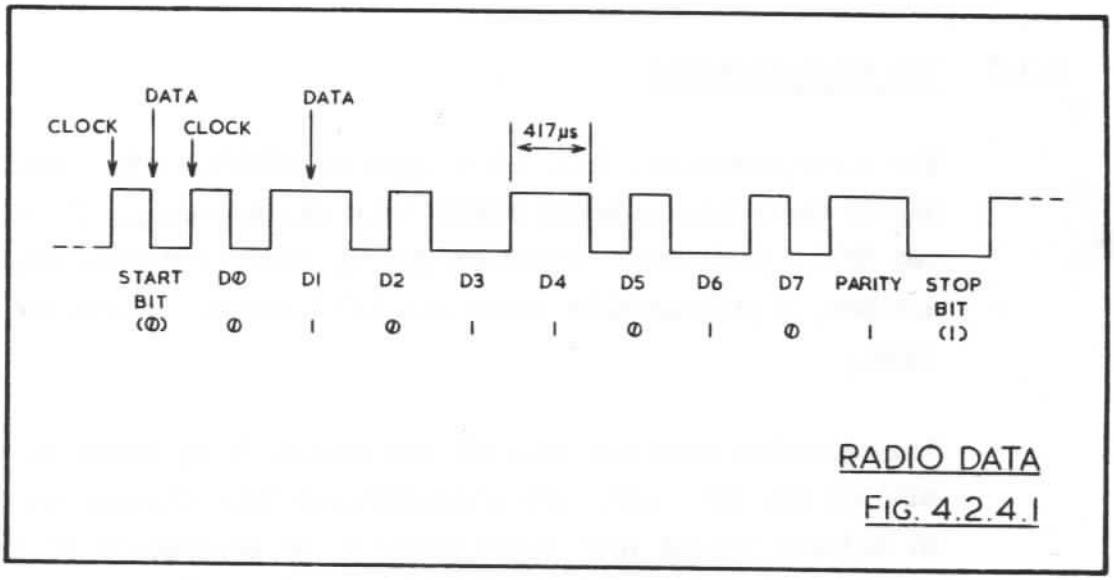
FIG. 4.2.3.1

Each infra-red data frame is preceded by a preamble, at least sixteen bits long, which consists entirely of data '1's. This is transmitted while the unit is testing the Rigger's Bus prior to transmission (see section 4.2.2). The first data '0' transmitted represents the start bit of the first data byte. Note that the Infra-red transmission takes place even if the unit is connected to

the Rigger's Bus and that all three transmissions (including Radio) occur almost simultaneously. Thus, if the Rigger's Bus is busy, the infra-red preamble will continue until it becomes free. If the unit is not connected to the Rigger's Bus, the preamble is always sixteen bits long.

4.2.4 Radio Transmissions

The radio output of the Designer's Control is a phase encoded audio signal intended for connection to a radio microphone or other, similar transmitter. The signal is similar in format to the Infra-red output, consisting of clock and data edges, the clock edges appearing at 417us intervals. Data 'Ø' is represented by an additional edge appearing between two clock edges. The form of the signal is shown in Fig. 4.2.4.1.



RADIO DATA
FIG. 4.2.4.1

As in the case of infra-red, each data frame is preceded by a preamble of data '1's, transmitted while the Rigger's Bus is being tested. The preamble is at least sixteen bits long.

4.3 DESIGNER'S CONTROL UNIT

Drawing No. 6A26662

4.3.1 Introduction

The Designer's Control consists of a battery powered, hand-held unit with a calculator-type keypad and LED display. At one end are mounted eight Infra-red emitting diodes, and connectors for the output to the Rank Strand Rigger's Bus and the input from the battery charger.

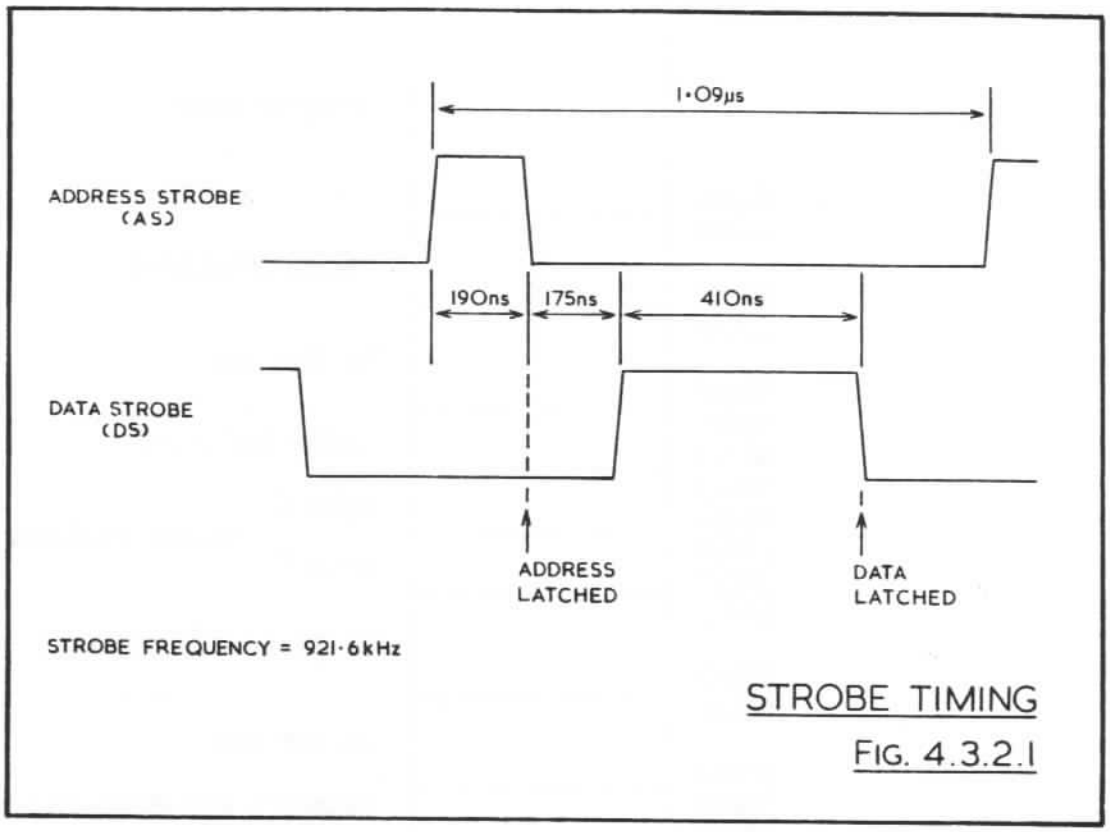
The majority of the unit electronics, and the keypad and display are mounted on a pair of printed circuit boards, linked by a flexible jump cable. These boards form a microprocessor system which is responsible for generating the Rigger's Bus and Infra-red outputs in response to keypad button actions.

4.3.2 The Microprocessor

The microprocessor, IC2, is a type MC146805E2 8-bit CMOS device - one of the Motorola M6805 family of microcomputers. It incorporates two 8-bit peripheral interface ports, used to detect keypad button actions, a programmable timer and 112 bytes of random access memory (RAM).

Communication with the rest of the system is by means of a five-bit address bus (A8 - A12) and a multiplexed Data/Address Bus (B0 - B7). An Address Strobe (AS) pulse permits the separation of the address signals (in latch IC5), to produce address lines A0 - A7. This gives a total available address space (including those addresses internal to the microprocessor, i.e. RAM, etc.) of 8Kbytes ($0000 - $1FFF). Correct data timing is ensured by a Data Strobe (DS) pulse.

The MPU derives the strobe signals from a 4.608MHz crystal, XL1, the output of which is divided by five to give a strobe frequency of 921.6kHz. The timing of the AS and DS signals is shown in Fig. 4.3.2.1.



STROBE TIMING

FIG. 4.3.2.1

4.3.3 Address Map

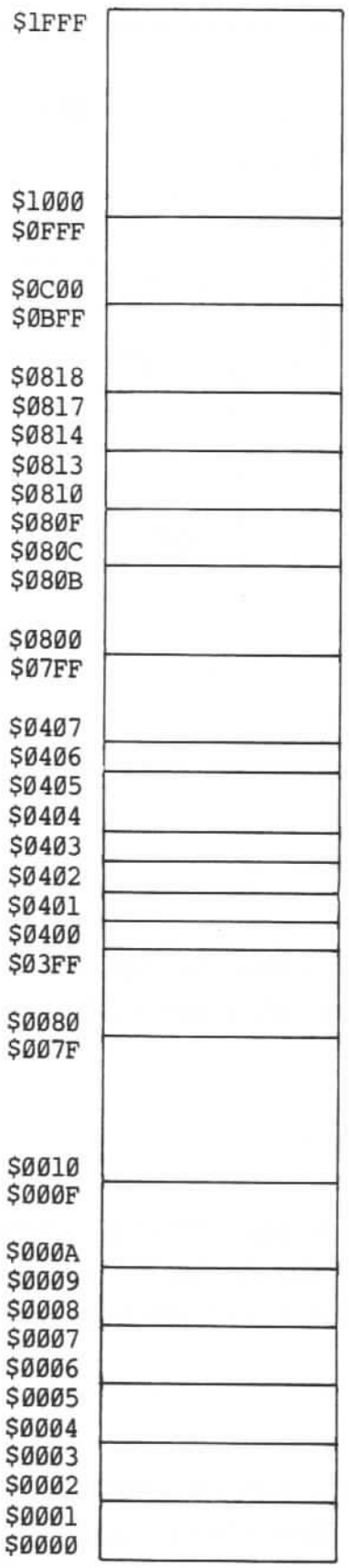
The system Address Map is shown in Fig. 4.3.3.1. Note that the addresses between $0000 and $007F are assigned to locations within the MPU.

4.3.3.1 Program ROM

The Program ROM, IC8, is a type MCM25L32 4Kbyte EPROM located at addresses $1000 to $1FFF. The device is selected by the low output of NAND gate IC7/11 when A12 and DS are both high.

4.3.3.2 Wheel Interface

A fourteen pin DIL socket, PL7, is provided for connection to a Galaxy type fader wheel. When fitted, this is located at addresses $0C00 -$0FFF. This facility is not used on the hand-held unit.



ADDRESS MAP

Fig. 4.3.3.1

4.3.3.3 Indicator Latch

The indicator LEDs on the keypad are driven by the outputs of an eight-bit latch, IC1, each indicator being on when the corresponding latch output is high. The latch receives data inputs from bus lines D0 - D7 and is clocked on the trailing edge of a negative-going pulse from pin 6 of decoder IC3. This pulse is produced each time the MPU writes to address $0817. The outputs of the latch may be disabled, thus turning off all the indicators, by a high output from pin 12 of addressable latch IC6 (address $0403 - see section 4.3.3.5).

The LEDs are arranged in two groups (bytes) enabled by the outputs of a flip-flop formed by IC7/3, IC7/6, VT2 and VT3. Byte 1 and byte 2 are respectively selected by accessing addresses $080C and $0810, thus producing a low output on either pin 4 or pin 5 of IC3, as appropriate. This sets the flip-flop into the required state. Note that four of the LEDs (LD12, LD11, LD1 and LD2) are common to both bytes and are enabled, via diodes D1 and D2, when either is selected.

4.3.3.4 Digital Display

The keypad display is formed by three 4-digit devices (DL2416) which receive display data, in ASCII code, from data lines D0 - D6. The required device is selected by the appropriate output of IC3 (pin 1, 2 or 3) whenever the MPU accesses addresses in the range $0800 - $080B. The digits within each device are selected by address lines A0 and A1, applied to pin 8 and 7 respectively, and a write pulse, applied to pin 6 (WR), from pin 7 of decoder IC12. The latter signal also enables decoder IC3. Note that the displays have a full alpha-numeric capability.

The displays are cleared on switch-on by the reset signal from C15/R23 and may be blanked by a low output from pin 11 of addressable latch IC6 (address $0402 - see section 4.3.3.5).

4.3.3.5 Output Latch

The outputs of the unit (Rigger's Bus and Infra-red) are generated by means of an addressable latch, IC6, which is selected when the MPU accesses addresses in the range $0400 - $0407. The latch is selected by the pin 6 output of decoder IC12 (applied to pin 4) which is used as a write pulse. The individual latches are selected by address lines A0 - A2 and the data input is from line D0 of the Data Bus.

Seven of the eight outputs from the latch are used, as follows:

i) Pin 9 (address $0400) - This pin provides the output to the Infra-red emitting diodes. The output signal is inverted by IC4/6 and applied to transistor VT1, which provides level conversion. The resulting 0V to +10V signal is routed via terminal 1 of connector PL6 to an FET which drives the Infra-red LEDs (see Drawing No. 7D26762).

ii) Pin 10 (address $0401) - This pin is used via VT6 and VT5 to drive the Rigger's Bus. When no transmission is in progress, the pin is high and VT5 is turned off. Under these circumstances the voltage on the bus depends on whether any other unit is transmitting. This may be tested as described in section vi below.

Before transmitting, the MPU checks that the bus is connected and not in use. If the bus is busy it is repeatedly tested until it has been free for about 7ms; i.e. long enough for the host system to detect that any previous transmission has finished. Transmissions then begin via IC6 pin 10. Each time the pin is set low, the Rigger's Bus is shorted by VT5 and this is detected at the host system receiver. The transmission format is described in section 4.2.

iii) Pin 11 (address $0402) - This pin is used to blank the digital display (see section 4.3.3.4).

iv) Pin 12 (address $0403) - This pin is used to disable the outputs of the indicator latch (see section 4.3.3.3).

v) Pins 13 and 14 (addresses $0404 and $0405) - These pins are used, via R42, R40 and C16, to produce a phase encoded output on terminal 2 of connector PL5. This signal is available for use in installations where a radio link is preferred to Infra-red.

vi) Pin 15 (address $0406) - This pin is used to test that the Rigger's Bus is connected and, if so, whether it is being used by any other unit.

When no unit is transmitting, the voltage on the bus is determined by termination resistors at the receiver in the host system. Under these circumstances +R equals +5V and -R equals 0V. If the bus is busy (i.e. if any unit is transmitting a '0') the +R and -R lines will be shorted together by the unit using the bus and they will both equal +2.5V.

The state of the bus is detected by transistors VT8 and VT7. If the bus is connected and not in use (+R = +5V, -R = 0V), both transistors are conducting and a low input is applied to pin 10 of NAND gate IC7/8. If the bus is not connected or a '0' is being transmitted, both transistors are off and IC7/8 pin 10 is high. The output of IC7/8 is connected to the IRQ input of the MPU.

The MPU tests the state of the bus by setting pin 15 of IC6 high, thus partially enabling IC7/8 on pin 9. If pin 10 of the gate is also high (bus busy or not connected) an interrupt request is generated on pin 2 of the MPU.

When the state of the bus has been read, the MPU resets IC6 pin 15.

4.3.3.6 Random Access Memory

The microprocessor incorporates 112 bytes of random access memory (RAM) which is located at addresses $0010 - $007F.

4.3.3.7 Timer

The MPU incorporates a software controlled timer which has two accessible registers located at addresses $0008 (Data Register) and $0009 (Timer Control Register). The timer is used to control transmission timing and the rate at which keypad contact scans take place.

4.3.3.8 Keypad Button Matrix

The MPU incorporates two 8-bit peripheral interface ports (A and B) which are used to detect keypad button actions. Each time the unit is switched on, the individual lines of Port A are programmed by the MPU as inputs and those of Port B as outputs. This is done by means of two Data Direction Registers located at addresses $0004 (A) and $0005 (B). The ports themselves are accessible to the MPU via two Data Registers located at addresses $0000 (A) and $0001 (B).

The keypad buttons are wired as an eight by four matrix with the eight rows connected to Port A and the four columns to lines PB0 - PB3 of Port B. To detect button actions, the MPU sets each column low in turn and reads the result via Port A. Where a key is operated, the appropriate row will be low, while otherwise the inputs are held high via resistors. The contacts are normally scanned once every 27.5ms. However, when the Rigger's Bus is being actively shared the time between scans will increase to about 33ms.

Lines PB4 - PB7 are connected to four system-configuration switches (SW33). The states of these are read via Port A in the same way as the keypad buttons. Note that the MPU only reads SW33 on power-up.

4.3.4 Address Decoding

Address lines A10 and A11 are decoded by IC12 to produce enable signals for the Wheel Interface ($0C00 - $0FFF), displays and indicators ($0800 - $0BFF) and Output Latch ($0400 - $07FF). The decoder is only enabled if A12 is low and DS high.

The displays and indicators enable signal (IC12 pin 7) is applied to a second decoder (IC3) which receives A2, A3 and A4. This is described in sections 4.3.3.3 and 4.3.3.4.

4.3.5 Power Supplies

The unit is powered by five AA-size quick-charge nickel-cadmium cells, from which are derived +5V and +10V rails. A socket is provided for connecting a 9V, 200mA battery charger.

Power is applied to the logic boards via connector PL6, terminals 4 (+V) and 2 (0V) and the positive rail is routed via switch SW2. The switched rail is applied to a voltage doubler circuit formed by IC11 and its associated components, and to a circuit which produces a +5V stabilised supply for the digital logic.

4.3.5.1 Voltage Doubler

IC11 contains an oscillator which connects pin 2 alternately between the switched rail and 0V. When pin 2 is at 0V, D7 is back-biassed and C12 charges via D6 to the level of the rail. Then, when pin 2 of IC11 is connected to the rail, the positive plate of C12 will move positively to a potential of approximately twice the rail voltage. D6 is thus back-biassed and C14 charges via D7. The voltage on C14 provides a rail at about +10V.

4.3.5.2 Logic Supply

The +5V logic supply is produced by a circuit formed by comparator IC10 and FET VT4. A +5.1V reference, derived from the +10V rail by zener diode D5, is applied to the non-inverting input of the

comparator and the supply is regulated by means of overall negative feedback.

4.3.5.3 Charging Circuit

The input from the battery charger is applied to the logic boards via terminal 3 of connector PL6 and is routed via current limiting resistor R11. Zener diode D4 limits the voltage across the batteries to 7.5V, to prevent overcharging.

4.3.6 Test Port

All of the MPU Address, Data and control signals appear on connector PL8, which is provided for the connection of a logic analyser or other test equipment.

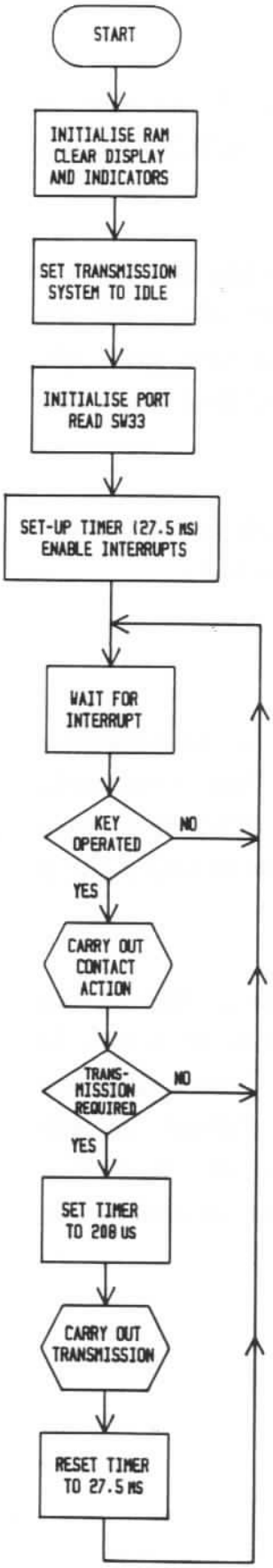
4.3.7 Designer's Control Program

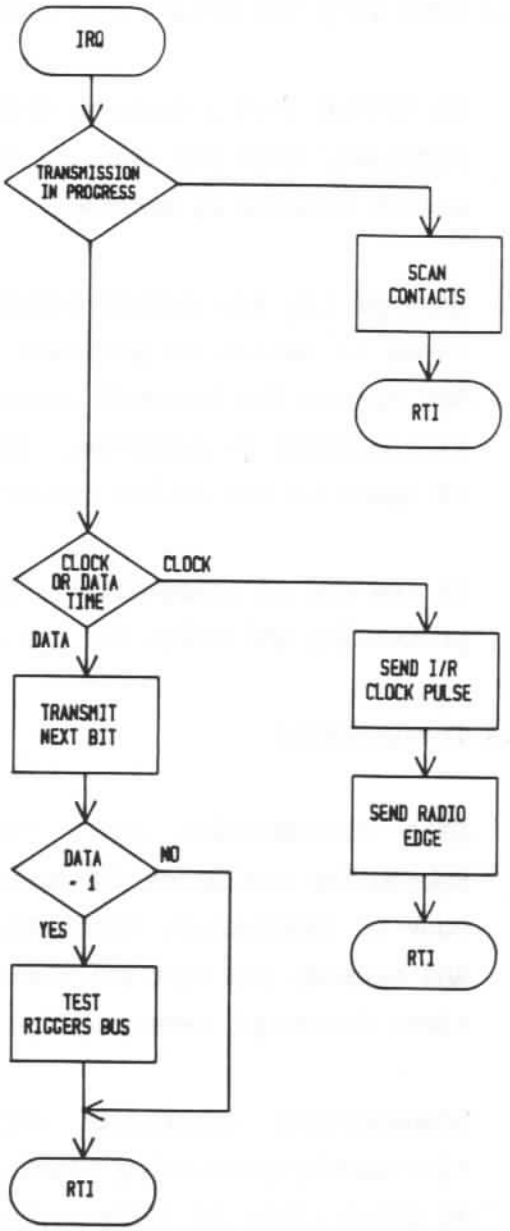
4.3.7.1 Initialisation

When the unit is switched on, the MPU initialises the RAM and clears the display and the indicators. It then sets the transmission system to the idle state, i.e. radio outputs in opposite states, infra-red equals '1', Rigger's output equals '1' and Rigger's Bus test disabled. The port is then set-up to scan the keypad button matrix (see section 4.3.3.8) and the settings of switches SW33 are read and stored. Finally the timer is set-up so that an interrupt request will be generated every 27.5ms (contact scan rate) and interrupts are enabled. The MPU then waits for an interrupt.

4.3.7.2 Contact Scan

Provided that a transmission is not in progress, a contact scan will take place each time the timer generates an interrupt request. The result of the scan is stored in the RAM and the MPU then returns from interrupt.





DESIGNERS CONTROL PROGRAM

FIG. 4.3.7

4.3.7.3 Base Loop and Action Routines

On return from a contact scan interrupt, the result of the scan is retrieved from RAM and, if a key was operated, the appropriate key action routine is entered.

Some of the key action routines will initiate a transmission. The timer is set-up to generate interrupt requests every 208us and the MPU enters the transmit subroutine. The latter continues until the transmission is complete. At the end of the transmission the timer is reset to the 27.5ms contact scan rate.

At the end of every action, or if no key was operated, the MPU stops processing and waits for the next timer interrupt request.

4.3.7.4 Transmission

Data transmission is a two level process. The transmission subroutine evaluates the state of the Rigger's Bus (not connected, busy or available), calculates the parity of the current data byte and sets-up the next bit for transmission. The MPU then waits for a timer interrupt (every 208us).

Transmission interrupts occur at twice the data bit rate, alternately generating clock and data signals. If the interrupt is at clock time, an infra-red clock pulse (5us) and a radio edge are transmitted. At data time the next data bit (set-up by the transmission subroutine) is transmitted and, if this bit is a '1', the Rigger's Bus is tested. The result of the latter is stored for evaluation on return from interrupt.

4.4 INFRA-RED RECEIVER

Drawing No. 6A26748

4.4.1 Introduction

The Infra-red receiver unit consists of a box fitted with a suspension bracket and an input horn. All of the electronic components (with the exception of the mains transformer) are mounted on a single printed circuit board attached to a removable front cover which also carries the input horn. The board is linked via multipin connectors to a terminal block in the body of the unit, which acts as a distribution point for input and output signals and power supplies (see Drawing No. 7C26761).

The receiver circuit comprises an infra-red detector, a radio (audio) input and a Rigger's Bus driver. The radio input provides an alternative mode of operation for use where infra-red is unsatisfactory (see Appendix).

4.4.2 Infra-red Input

The Infra-red signal from the Designer's Control is received on an array of 16 photo-diodes mounted behind a special infra-red filter. The latter helps prevent the infra-red signal being swamped by ambient light. The signal produced by the photo-diodes is applied to a low-noise pre-amplifier formed by FET VT1 and transistors VT2, VT3 and VT4. Negative d.c. feedback via R6 and R7 gives this amplifier a gain of about 1Ø, while low-frequency roll-off is provided by C3 and R5.

The output of the pre-amplifier, taken from the emitter of VT4, is routed via inverting Op-amp IC1 (which has a gain of about 2Ø) to a bandpass filter formed by IC2 and IC3 and their associated components. This filter is centred on 5ØkHz and has a low Q, allowing a step response to be passed. The output from IC3 is in turn applied to a high-pass filter, formed by IC4 and its associated components, which ensures a negligible response to signals at mains frequency and its lower-order harmonics.

The output of IC4 is applied, via preset potentiometer RV1 (sensitivity control), to threshold detector IC6. The threshold is set by resistors R46, R47 and R61. Note that once the preamble has been received, the threshold of IC6 is reduced by a low output from IC11/13, applied via R61.

4.4.3 Radio Input

On systems using radio instead of infra-red, the input from the radio receiver is connected to terminals 2 and 1 of PL3 and applied, via C37, to the input of pre-amplifier IC9. This has a gain of about 6, set by sensitivity control RV2, and its output is applied to comparators IC8/13 and IC8/14.

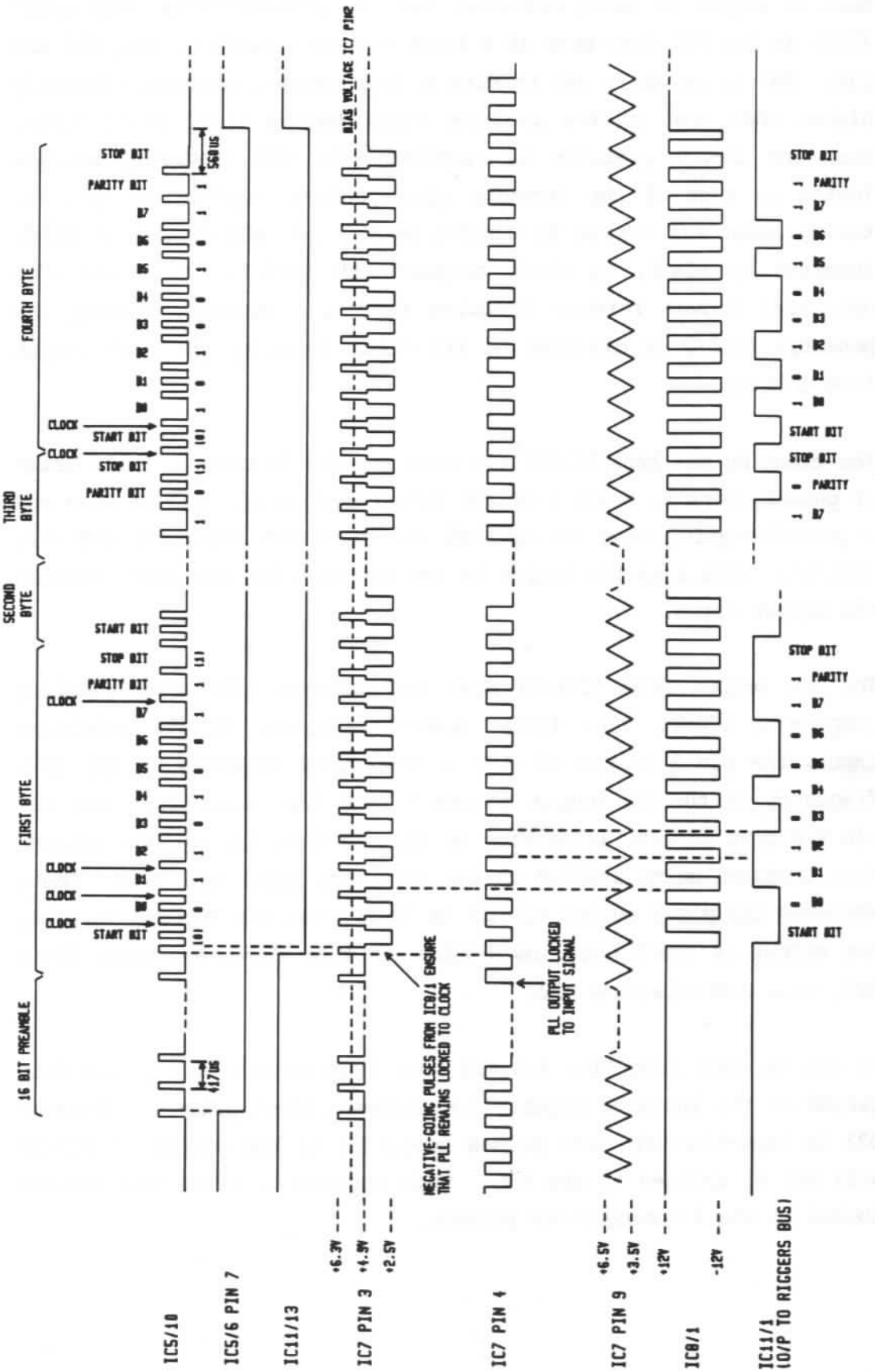
A four volt window, centred on 0V, is defined by potential dividers R42/R39 and R34/R33, and pulses at the output of IC9, limited to +/-4V, are compared with this window by the two comparators. If either the upper or the lower threshold is exceeded, the appropriate comparator produces a low output, thus pulling down the junction of R32 and R31. The switch action of each comparator is improved by a small amount of hysteresis introduced by means of positive feedback.

4.4.4 Output to Rigger's Bus

The outputs from IC6, IC8/13 and IC8/14 are combined at the trigger input of monostable IC5/10. On the negative-going edge of the appropriate signal, IC5/10 fires and produces a 100us positive-going pulse which is applied to phase-locked-loop (PLL) IC7 and counter IC10.

4.4.4.1 Phase-Locked-Loop

The pulses from IC5/10 are applied via D22 and R49 to pin 3 of IC7, while a reference voltage is provided on pin 2 by a potential divider formed by R52, R50 and R51. At the start of the preamble, the output of IC11/13 is high and this pulls up the non-inverting input (pin 7) of IC8/1 via D23, ensuring that the output of the latter device is high and D25 is back-biassed.



INFRA-RED RECEIVER - OUTPUT WAVEFORMS

FIG. 4.4.4.1

When no signal is being received, the Voltage-Controlled Oscillator (VCO) in the PLL free-runs at a frequency determined by RV3, R27 and C30. RV3 is normally set to give a free-running frequency slightly higher than that of the incoming clock pulses (i.e. about 2kHz). When the 16-bit preamble is received, the VCO frequency becomes locked to that of the incoming clock pulses (applied to pin 3), taking about six cycles to achieve lock. The VCO output is used, inverted by IC8/6, to clock output-latch IC11/1, the clock edge occurring midway between incoming pulses. However, during the preamble IC11/1 is disabled on its clear input by the high output from IC11/13.

The clock pulses from IC5/10 are also applied to counter IC10. After 16 pulses, pins 5, 6 and 7 of the latter device will all be high and a positive-going edge is applied to the clock input of bistable IC11/13. This sets the output of the bistable low and thus releases the output latch.

The low output from IC11/13 also back-biasses D23, thus enabling comparator IC8/1. The latter device receives, on its inverting input, the pin 9 output of IC7; a triangular waveform at the same frequency as the VCO output on pin 4 (see Fig. 4.4.4.1). The IC7 pin 9 output is also integrated by R53 and C35, the average voltage thus produced being applied to the inverting input of IC8/1. Thus, whenever the pin 9 output of IC7 is lower than its average voltage, the output of IC8/1 goes low (-12V) and this forward-biasses diode D25, thus back-biassing D22.

It can be seen from Fig. 4.4.4.1 that this occurs during the data period of the incoming signal (i.e. between clock pulses). Because D22 is back-biassed, data pulses appearing on the output of IC5/10 will not be applied to the PLL. This ensures that the VCO remains locked to the incoming clock pulses.

4.4.4.2 Rigger's Bus Output

The Rigger's Bus is driven by FET VT5, which is controlled by the pin 1 output of bistable IC11/1. The latter device receives the clock and data pulses from IC5/10 on its data input (pin 5) and is clocked on pin 3 by the inverted VCO output from IC7 (pin 4). The clock edges occur during the data period (i.e. midway between clock pulses) of each bit received.

For each data '0' received, IC5/10 produces a pulse which, applied to IC11/1, causes the output of the bistable to be set high. This switches on VT5 and shorts the Rigger's Bus lines. For a data '1', this pulse is absent and IC11 pin is set low, switching off VT5.

Note that there is no provision for testing the state of the Rigger's Bus which may therefore not be shared by another control unit.

4.4.4.3 Transmission-in-progress Monostable

At the beginning of each transmission, the first clock pulse from IC5/10 trigger's monostable IC5/6. The latter device has a period of 560us, but is retriggered by each clock and data pulse, thus producing an output for the whole of the transmission. The pin 7 output of IC5/6 enables counter IC10 and bistable IC11/13, while pin 6 drives transistors VT6 and VT7, thus illuminating LED1 which indicates that a transmission is being received.

At the end of a transmission, or if a transmission should be interupted, IC5/6 will time-out, thus resetting IC10 and IC11/13. IC11/13 in turn disables output-latch IC11/1.

4.4.5 Power Supplies

The printed circuit board is powered from a transformer, separately mounted within the unit (see Drawing No. 7C26761). This has two 15V secondary windings and its primary winding is protected by a 2A HRC fuse (3.15A on 120V systems).

The transformer output is connected to the printed circuit board via connector PL2 and, after full wave rectification and smoothing, is applied to two integrated circuit regulators, REG1 and REG2. These respectively provide +12V and -12V rails, while the junction of the two transformer secondary windings gives a central 0V rail. The d.c. supplies are protected by 1A fuses in the outputs from the bridge rectifier.

Fused +/-20V outputs (taken via connector PL1) permit up to six receiver units to be connected together, only a single mains connection then being necessary. If screened 4-core cable is used, this may also carry the Rigger's Bus. The individual conductors should not be smaller than $0.5mm^2$.

CHAPTER 5

MAINTENANCE

5.1 INTRODUCTION

This chapter provides details regarding the initial setting-up of the equipment, fuse replacement and the means of access to components, etc.

Note: The Designer's Control and Infra-red Receiver contain few user-replaceable parts. Repairs should only be carried out by a qualified engineer authorised to maintain this equipment.

5.1.1 Equipment Required

The following equipment is required in order to maintain the system:

i) Multi-meter

This should be capable of measuring up to 5ØV d.c. at 1A with an accuracy of 1% of displayed value, and up to 25ØV a.c. (5ØHz) at 1ØA with an accuracy of 5% of displayed value.

ii) Oscilloscope

The oscilloscope should be a dual-trace type capable of measuring signals of ØV to 15V d.c., and ØV to 11Ø/24ØV a.c. It should have a time-base range from <1Øns to >3 secs.

iii) Oscillator This should have a square-wave output with the frequency adjustable to greater than 1ØØkHz and the output level adjustable from ØV to +5V.

iv) Solder Remover

This should be of the 'suction' type.

v) Soldering Iron

This should be of a temperature-controlled type, with a maximum temperature not greater than 370 degrees Celsius.

See also section 5.2.2.1.

5.1.2 General Cautions

5.1.2.1 Power

The Infra-red Receiver is powered from either a 110V or a 240V a.c. source. **THIS VOLTAGE CAN BE FATAL.** Whenever the power terminals are exposed, the technician should be insulated from ground (preferably using a rubber mat).

5.1.2.2 Proms

Erasable Programmable Read Only Memories must not be exposed to direct sunlight or to ultra-violet light. Continuous exposure may destroy the program content.

5.1.2.3 Handling CMOS Integrated Circuits

CMOS DEVICES ARE DESTROYED BY STATIC ELECTRICITY. When handling these integrated circuits, ensure that YOU and THE BENCH are at the same potential. Failure to do so could result in damage to the IC. A convenient method of achieving this is to use a copper ring which fits one finger and arrange a flexible wire which incorporates a 1M0 resistor from the ring to the bench, the surface of which should be earthed metal. Note that this procedure must not be adopted when hazardous voltages are present.

Always ensure that integrated circuits remain in their wrapping until you need them - never leave them un-earthed (the wrapping 'earths' all the pins, avoiding capacitatively induced voltage).

Under no circumstances should such devices be stored in polythene or other high static containers.

5.1.2.4 Food and Drink

Food or drink should not be consumed in the immediate vicinity of the equipment. Drinks, especially those containing sugar, could cause irreparable damage, apart from the possibility of short-circuiting the power supplies.

5.2 INITIAL SETTING-UP

5.2.1 Designer's Control Unit

The Designer's Control operational parameters are entirely determined by the host system and there are no options which may be selected by the user. However, units are available with additional operational facilities and, should it be necessary to change the printed circuit boards for any reason, the settings of switches SW33 should be checked. The valid settings are as follows:

SW33/1-2 - i) On units without Pan, Tilt and Focus (PTF) facilities (i.e. standard Designer's Control) both switches should be set Off.

ii) For units with limited PTF (i.e. without Hoist and Barn Door control), set SW33/1 On and SW33/2 Off.

iii) For units with full PTF, set SW33/1 Off, and SW33/2 On.

SW33/3 - On units with PTF facilities, certain control functions cause alphabetic strings to appear in the display window. These may be in English or German, depending on the setting of SW33/3: Off for English, On for German.

SW33/4 - This switch is not used, but should be set Off.

Note that the settings of SW33 are only read by the microprocessor on power-up and that, if the settings are changed while the unit is switched on, this will have no effect until the unit is switched Off and On again.

5.2.2 Infra-red Receiver

The Infra-red Receiver has three preset potentiometers which have the following functions:

RV1 - Infra-red sensitivity control.

RV2 - Radio sensitivity control: Unless the radio facility is being used, RV2 should be turned fully anticlockwise (working from the component side of the board). When using radio, set RV1 fully anticlockwise and RV2 as described in the Appendix.

RV3 - VCO frequency control.

5.2.2.1 General

An oscilloscope and a square-wave oscillator are required when setting-up a Designer's Control Infra-red Receiver (see section 5.1.1). Also required are the following:

1) 100R resistor.

2) 1k0 resistor.

3) TIL38 infra-red light emitting diode.

4) 60W mains-powered incandescent lamp.

5) Designer's Control.

Optimum performance of the Designer's Control Receiver depends on the the signal-to-noise ratio within the infra-red receiving circuits. During adjustment, therefore, care must be taken to avoid the introduction of noise signals. The following are particularly important:

a) The test bench must be tidy.

b) Ambient fluorescent lighting should be reduced as much as possible.

c) The receiver PCB must be securely earthed to the receiver front panel throughout the adjustment procedure.

d) All test probes must be locally earthed to the PCB.

5.2.2.2 Receiver Front-end Checks

1) Open the receiver.

2) Connect the oscilloscope probe to IC14 pin 6 and the earth clip to ØV. Observe the background noise (expected value: about 500mV peak-to-peak under normal lighting conditions; if greater than 1V peak-to-peak reduce the ambient lighting).

3) Solder the 100R resistor across the photo-diode array. Observe the background noise (expected value: below 25mV peak-to-peak; a value higher than this indicates a fault condition).

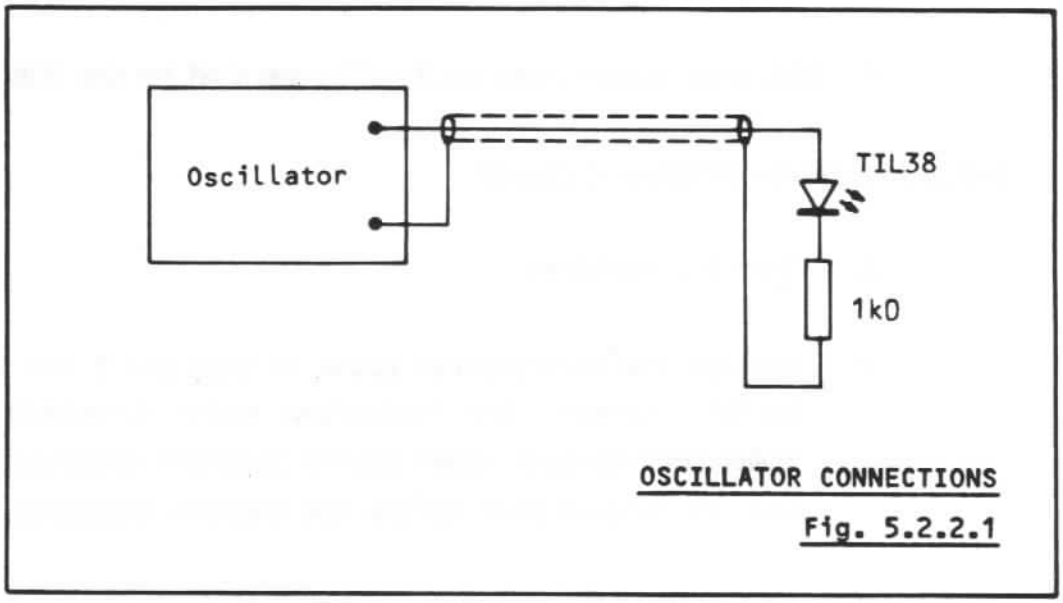
4) Remove the 100R resistor. Switch on the 60W lamp and place it 1 metre from the front of the receiver. Observe the noise (typical value: 1-1.5V peak-to-peak with no mains frequency component present; presence of mains frequency indicates a fault condition).

5) Move the lamp progressively closer to the receiver. Mains frequency interruptions in the noise should become noticeable and the receiver will eventually overload and 'lock out'. The

d.c. level across RV1 should remain constant at ØV; if any variation is seen a fault condition is indicated.

6) Connect the 1KØ resistor and the TIL38 LED to the oscillator as shown in Fig. 5.2.2.1. Monitor the voltage across the resistor and adjust the output of the oscillator until a 1V peak-to-peak square wave is measured. Position the LED 300mm in front of the photo-diode array.

Note: Do not hold the LED in place by hand. Keep the oscillator and cable well clear of the receiver.



OSCILLATOR CONNECTIONS

Fig. 5.2.2.1

7) Monitor the signal at IC4 pin 6 and adjust the oscillator frequency for maximum signal level. Correct operation is indicated by the following:

a) The signal should be sinusoidal.
b) The maximum value should be obtained between 100kHz and 120kHz.
c) The maximum should have a value of at least 4V peak-to-peak.

d) A value of at least 4V peak-to-peak should be obtained between 1Ø8kHz and 112kHz.

e) Adjusting the frequency to 25kHz above or below the frequency at which the maximum is obtained should cause a fall in signal level to 2V peak-to-peak.

If a badly distorted signal is observed or if any of the other conditions is not fulfilled, a fault condition is indicated.

5.2.2.3 Demodulator Adjustment

1) Place a transmitter next to the receiver and transmit a continuous signal (e.g. channel 1 fade up). Trigger the oscilloscope off the signal (not off the noise) at IC4 pin 6.

2) Set RV1 fully anti-clockwise (adjusting from the component side of the board) and RV3 fully clockwise. Monitor IC11 pin 3 and adjust RV3 slowly until a clock signal is observed on the oscilloscope. Adjust RV3 until the clock frequency is about 2% slower than the received signal (which is being used as a trigger).

3) Turn RV1 slowly clockwise; the clock should 'lock' to the incoming signal.

4) Cease transmission of data.

5) Connect one oscilloscope input to IC6 pin 2 and the other to IC6 pin 3. Adjust the oscilloscope display so that the ØV d.c. levels of the two traces coincide. Adjust RV1 until the level of the broadband noise is half the comparator threshold; noise spikes of up to +3dB can be ignored.

5.2.2.4 Final Checks

1) Blank out all but one forward facing LED on the transmitter.

2) Transmit at a range of 3.5 metres. Measure the signal at IC4 pin 6 (expected value: 20V peak-to-peak; a markedly lower level indicates a fault).

3) Repeat at a range of 7 metres (expected value: 10V peak-to-peak).

4) Repeat at a range of 14 metres (expected value: between 3.6V and 5V peak-to-peak).

5) Close the unit and check operationally with a Memory Lighting system.

5.3 ROUTINE SERVICING

Very little routine servicing is necessary, apart from keeping the equipment clean and the batteries charged. To clean, use a lint-free anti-static cloth or, in the case of persistent marks, a SMALL amount of anti-static cleaner. Do not use any other type of cleaner as scratching or discoloration may result. Note that if the Infra-red facility is being used, particular attention must be paid to the infra-red LEDs on the control unit and the infra-red filter on the receiver(s).

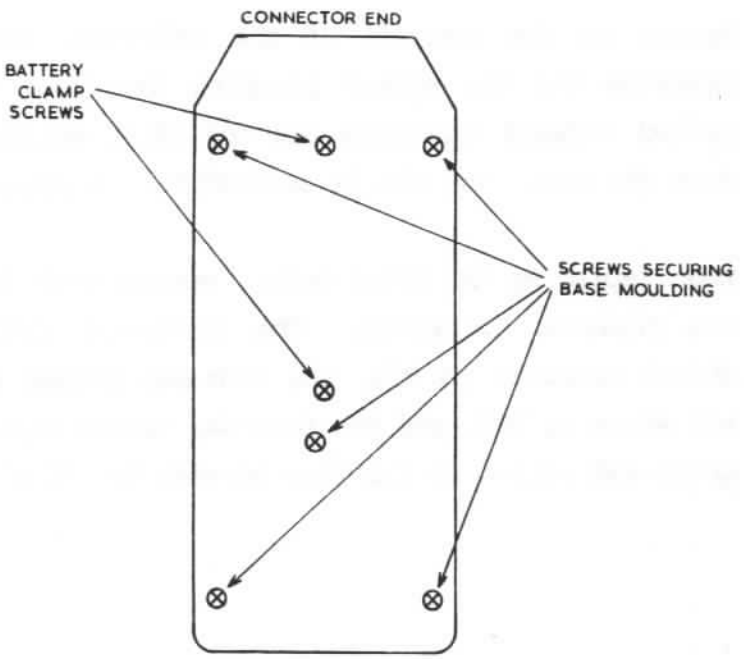
5.4 FUSES

No fuses are fitted on the Designer's Control unit, but the Infra-red receiver has fuses protecting the mains input and the +20V and -20V d.c. supplies. The mains fuse is 2A HRC (or 3.15A HRC on 120V systems) and the two d.c. fuses are rated at 1A.

5.5 REMOVAL AND REFITTING OF SUB-ASSEMBLIES

5.5.1 Designer's Control

Access to the interior of the Designer's Control unit is obtained by removing the five screws securing the base moulding. Do not remove the two screws which hold the battery clamp (see Fig. 5.5.1.1). Lift off the base moulding carefully, so as not to damage the wiring to the batteries.



DESIGNER'S CONTROL - REAR VIEW

FIG. 5.5.1.1

The above gives access to the rear of the PCB assembly and to connector PL8 (for the connection of a logic analyser or other test equipment). To remove the PCB assembly, first disconnect the two multiway connectors (PL5 and PL6) and then remove the pillars at the four corners of the PCB. The PCBs may now be carefully lifted out.

The two halves of the PCB assembly may be separated after removing the central pillar. The boards hinge about the multiway jump cable, which must be treated with care to avoid damage.

Re-assembly is the reverse of the above procedure. When replacing the printed circuit boards, ensure that the indicator LEDs and keypad push-buttons align correctly with the holes in the control panel. Also, care must be taken when fitting the base moulding so that none of the battery cables, etc. are trapped and damaged.

5.5.2 Infra-red Receiver

Access to the interior of the Infra-red Receiver is obtained by removing the six screws securing the front cover. This should be pulled forward carefully and the three multiway connectors removed from the PCB. The PCB is secured to the front cover by four nuts.

When replacing the front cover, ensure that the multiway connectors are replaced correctly. The three-way socket (green, orange and white) connects to PL1, the four-way socket with wires coded green and slate to PL2, and the four-way socket with wires coded red, blue green and yellow to PL3 (see Drawing No. 7C26761).

APPENDIX

NOTES ON USING A RADIO LINK

A1 INTRODUCTION

If desired, a radio microphone system may be used for the Designer's Control data link, instead of the standard Rigger's Bus or Infra-red link. When this facility is used, a single Infra-red receiver is necessary to act as an interface between the radio receiver and the Rigger's Bus input of the host system.

When correctly set-up, the radio link should have a range comparable with that obtained using the radio microphone conventionally.

A2 TRANSMITTER

The Designer's Control produces a phase-encoded signal at line level on pin 5 of the XLR connector, the return being on pin 3 (see Drawing No. 7D26762). This signal should be reduced to a suitable level by means of a potential divider at the input to the transmitter. Suitable values for a low impedance dynamic input are 10kØ for the input resistor and 220R for the shunt resistor. The signal level at the transmitter must not be too high or the operation of the modulation limiter circuits will cause data errors. This may be observed by connecting an oscilloscope at the output of the receiver. If the transmitter is being over-driven, the output pulses towards the end of each data frame will appear truncated.

A3 RECEIVER

The output from the radio receiver should be connected to terminal 5 on the terminal block inside the Infra-red Receiver unit, with the return on terminal 6 (see Drawing No. 7C26761). The signal should be at line level, the headphone monitor output of the radio receiver being a suitable source.

Because of the lack of d.c. restoration, the radio receiver output will 'ring' at the end of each data frame. The duration of this is determined by the low frequency response of the receiver, the output impedance and the signal level. Optimum results will be obtained with the signal level as high as possible, but with an end-of-transmission 'ring' not longer than 9ms. This may be adjusted by means of potentiometer RV2 on the infra-red receiver board and is best set using an oscilloscope connected to the output of IC9. Should an oscilloscope not be available, increase the setting of RV2 (clockwise) until data errors occur and then turn it slowly back to the point where the data received is again error free.

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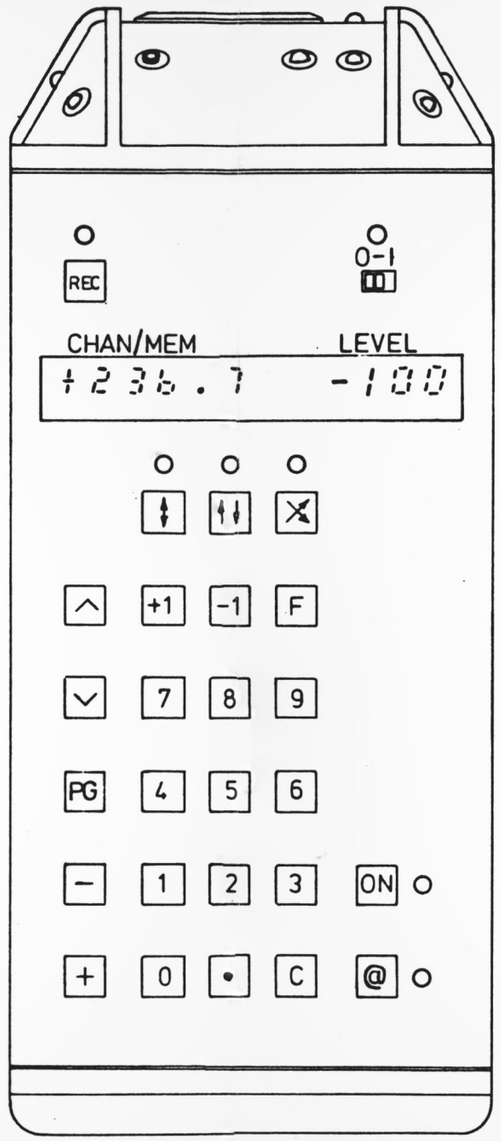
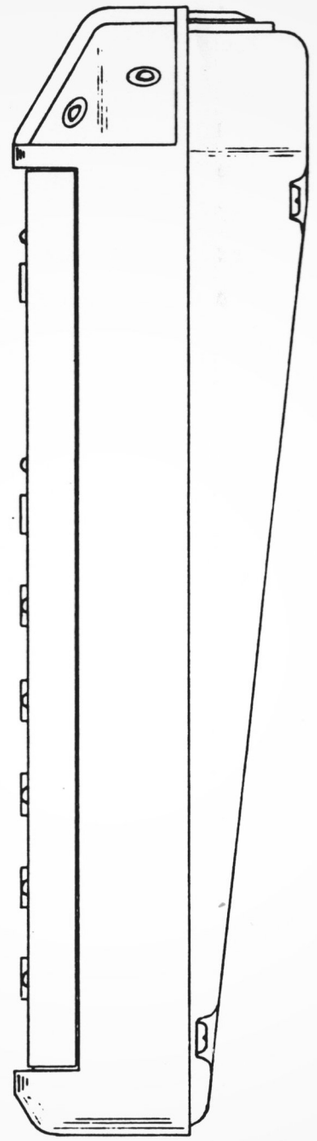
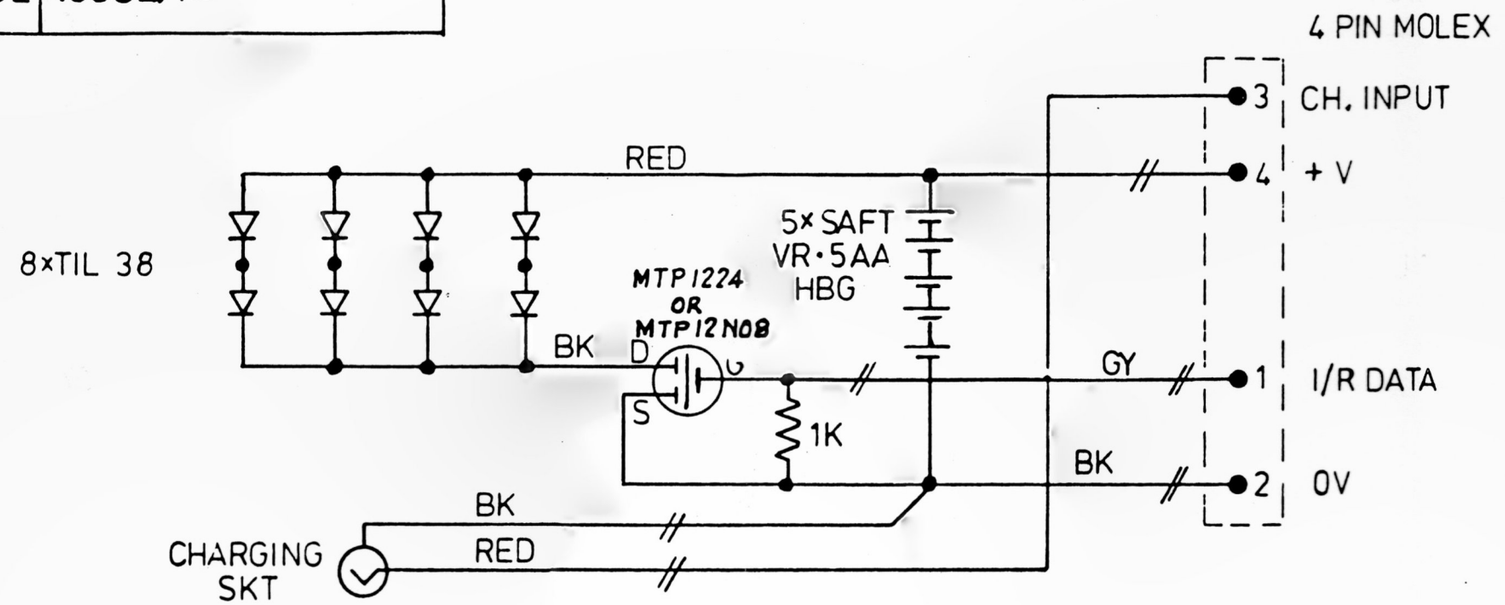




REV.1. C.N.º	**RANK STRAND ELECTRIC** PO Box 51 Great West Road Brentford Middlesex TW8 9HR Telephone 01-568 9222 Telex 27976 A DIVISION OF **RANK AUDIO VISUAL LIMITED**	TOLERANCES IMPERIAL / METRIC FRACTION ± 1/64" / 1 DEC PLACE ± 0·4mm DECIMAL ± ·005" / 2 DEC PLACE ± 0·1mm ANGULAR ± 0·25° UNLESS OTHERWISE STATED USED ON :- IL 26800	SCALE 1:1 DATE DRAWN V.G.P. 8/1/82 CHECKED 7-5-82 APPROVED 7·5·82. MATERIAL :- FINISH :-	TITLE :- DESIGNERS CONTROL LAYOUT (HAND HELD)	
	DIMENSIONS IN INCHES/MILLIMETRES THIRD ANGLE PROJECTION			ISSUE A	DWG. Nº 1C 26694

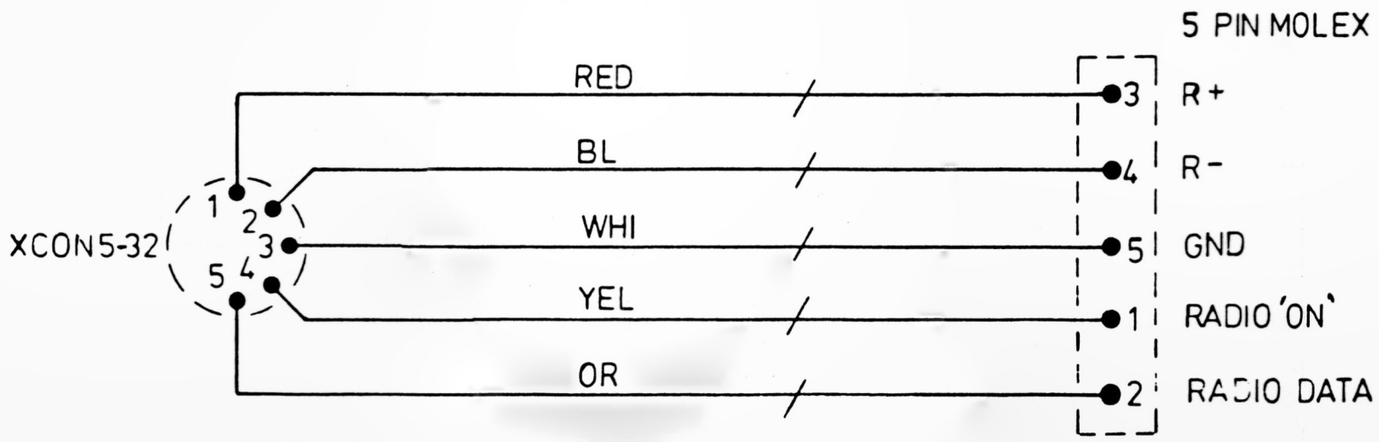
WW:99

DWG. Nº 7D 26762	ISSUE A B



NOTE

BATTERIES TO BE LEFT UN CONNECTED UNTIL TEST



WIRING

0·08mm²

0·2mm²

REMAINDER 1·0mm²

REV.1. C.Nº E6003
MTP12N08 ADDED AS ALTERNATIVE.
20/6/83. 21/6/83

RANK STRAND ELECTRIC

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Rank Audio Visual Limited

DIMENSIONS IN INCHES/MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES	
IMPERIAL	METRIC
FRACTION ± 1/64"	1DEC PLACE ± 0·4mm
DECIMAL ± ·005"	2DEC PLACE ± 0·1mm
ANGULAR ± 0·25°	
UNLESS OTHERWISE STATED	

USED ON :- IL 26800

		DATE
SCALE		
DRAWN	V.G.R.	5/3/82
CHECKED		7-5-82
APPROVED		7-5-82.

MATERIAL:-

FINISH:-

TITLE:-

WIRING DIAGRAM

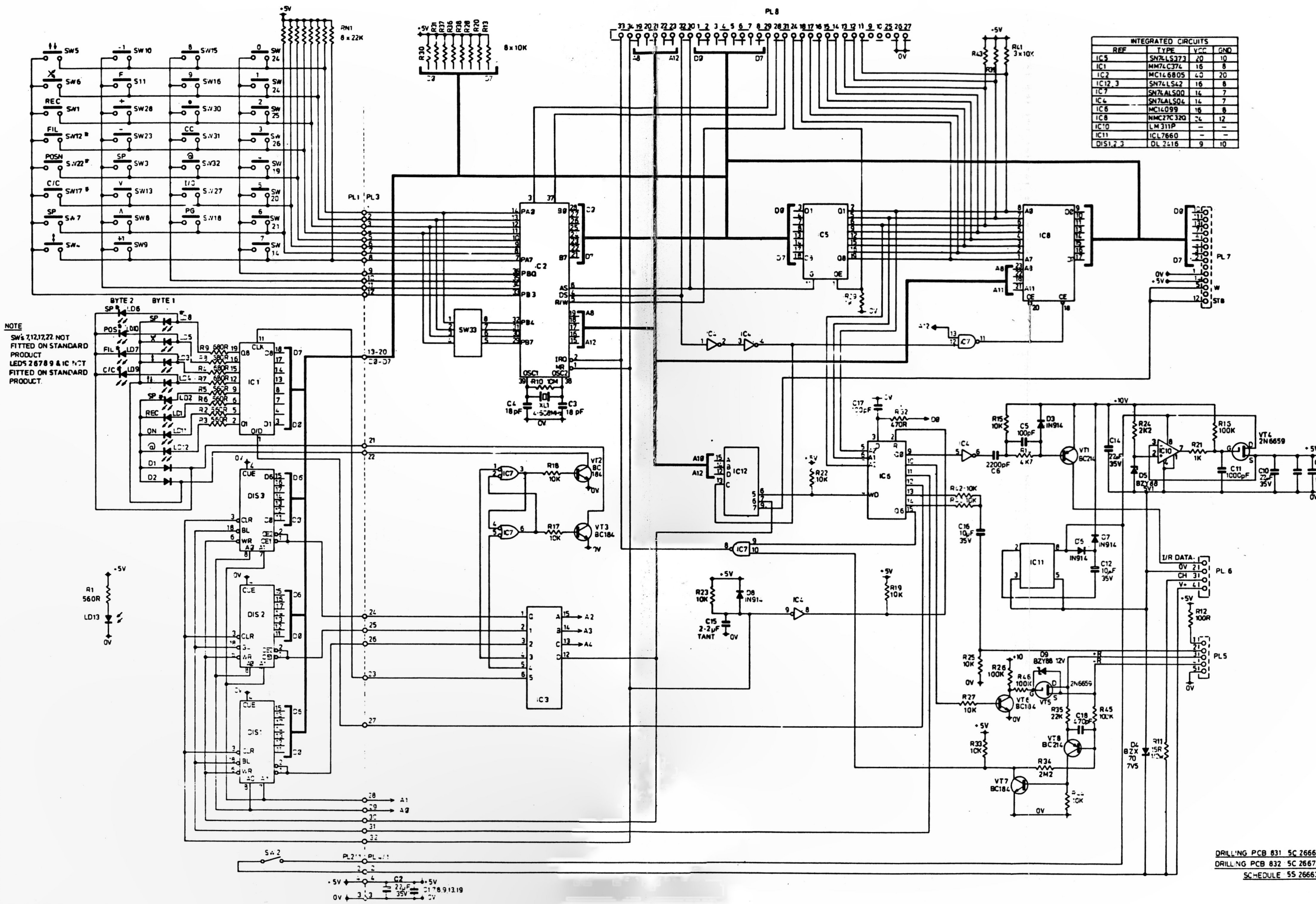
HAND HELD DESIGNERS CONTROL

ISSUE A B

DWG.Nº 7D 26762

PS 824

DWG. Nº 6A26662 | ISSUE E



NOTE
SW's 7,12,17,22 NOT FITTED ON STANDARD PRODUCT
LEDS 2,6,7,8,9 & 10 NOT FITTED ON STANDARD PRODUCT.

INTEGRATED CIRCUITS			
REF	TYPE	VCC	GND
IC5	SN74LS373	20	10
IC1	MM74C374	16	8
IC2	MC146805	40	20
IC12, 3	SN74LS42	16	8
IC7	SN74ALS00	14	7
IC4	SN74ALS04	14	7
IC6	MC14099	16	8
IC8	NMC27C32Q	24	12
IC10	LM311P	–	–
IC11	ICL7660	–	–
DIS1,2,3	DL 2416	9	10

DRILLING PCB 831 5C 26664
DRILLING PCB 832 5C 26672
SCHEDULE 5S 26663

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DIMENSIONS IN INCHES/MILLIMETRES
THIRD ANGLE PROJECTION

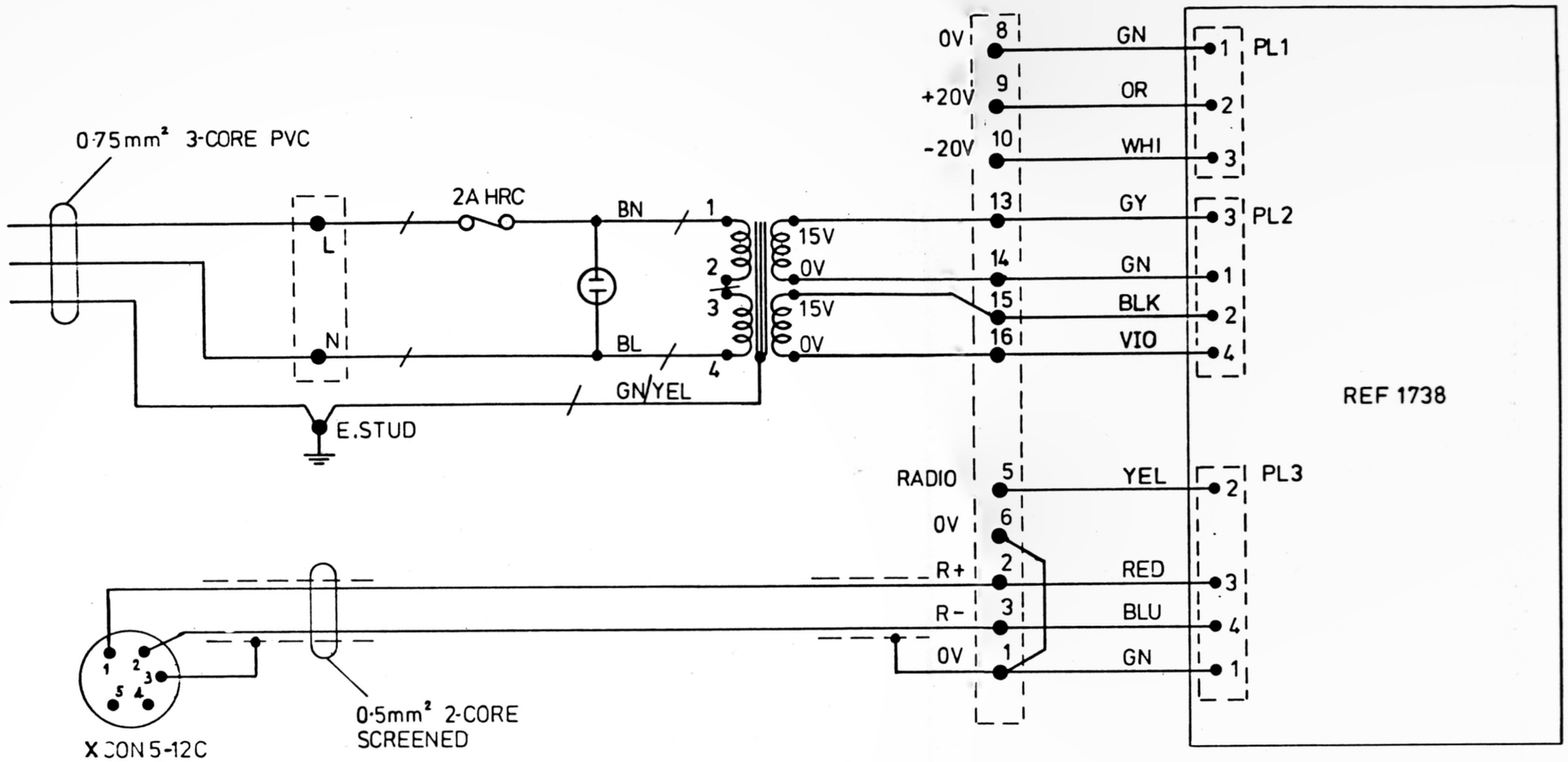
TOLERANCES
IMPERIAL: FRACTION ± 1/64" ; DECIMAL ± .005"
METRIC: 1 DEC PLACE ± 0.4mm ; 2 DEC PLACE ± 0.1mm
ANGULAR ± 0.25°
UNLESS OTHERWISE STATED

USED ON:- DESIGNERS CONTROL 1L 26800

SCALE | DRAWN | CHECKED | APPROVED | DATE
MATERIAL:-
FINISH:-

TITLE:- DESIGNERS CONTROL - EMITTER
PCB 831/3 832/4
REF 1733A / B
ISSUE E
DWG. Nº 6A26662

DWG. Nº 7C 26761	ISSUE AB

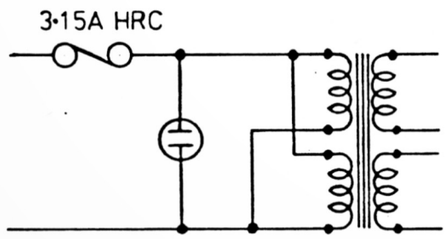


NOTE

ENSURE REF 1738 EARTH PLANE IS BONDED TO BOX LID VIA THE TOP TWO FIXING STUDS.

WIRING — 1·0mm²

REMAINDER 0·2mm²



120V WIRING

REV.1. C.Nº E8550
TERMINALS 15 and 16 WIRE COLOURS WERE GREEN and GREY
[illegible] 16-1-86
[illegible] 16-1-86

WW 289

RANK STRAND ELECTRIC
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DIMENSIONS IN INCHES/MILLIMETRES
THIRD ANGLE PROJECTION

TOLERANCES	
IMPERIAL	METRIC
FRACTION ± 1/64"	1 DEC PLACE ± 0·4mm
DECIMAL ± ·005"	2 DEC PLACE ± 0·1mm
ANGULAR ± 0·25°	
UNLESS OTHERWISE STATED	

USED ON :- IL 26800

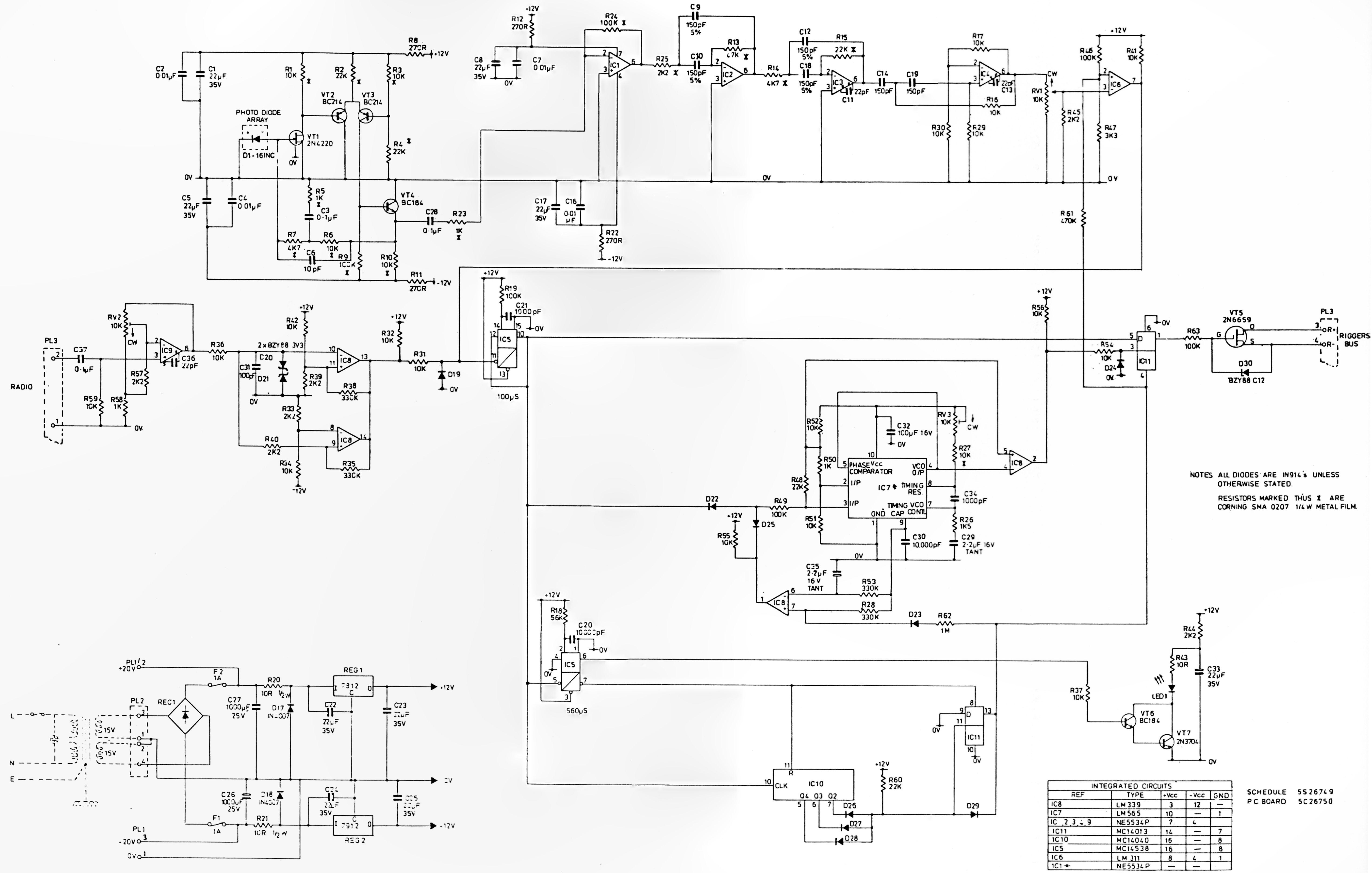
		DATE
SCALE		
DRAWN	V.G.P.	5/3/82
CHECKED	[illegible]	7-5-82
APPROVED	[illegible]	7-5-82.
MATERIAL :-		
FINISH :-		

TITLE :-

DESIGNERS RECEIVER WIRING DIAGRAM

ISSUE AB | DWG. Nº 7C 26761

DWG. Nº 6A26748 | ISSUE ØØØE



NOTES ALL DIODES ARE IN914's UNLESS OTHERWISE STATED.

RESISTORS MARKED THUS ✗ ARE CORNING SMA 0207 1/4W METAL FILM.

INTEGRATED CIRCUITS				
REF	TYPE	+Vcc	-Vcc	GND
IC8	LM339	3	12	—
IC7	LM565	10	—	1
IC 2,3,4,9	NE5534P	7	4	
IC11	MC14013	14	—	7
IC10	MC14040	16	—	8
IC5	MC14538	16	—	8
IC6	LM 311	8	4	1
IC1 •	NE5534P	—	—	

• REFER TO CIRCUIT.

SCHEDULE 5S26749
P C BOARD 5C26750

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DIMENSIONS IN INCHES/MILLIMETRES
THIRD ANGLE PROJECTION

TOLERANCES	
IMPERIAL	METRIC
FRACTION ± 1/64"	1 DEC PLACE ± 0.4
DECIMAL ± .005"	2 DEC PLACE ± 0.1
ANGULAR ± 0.25°	
UNLESS OTHERWISE STATED	

USED ON :- 1L26800

SCALE	—	DATE
DRAWN	G HAYWARD	23 2 82
CHECKED		
APPROVED		

MATERIAL :-

FINISH :-

TITLE :- DESIGNERS CONTROL RECIEVER

PCB842/2

REF 1738

ISSUE ØØØE

DWG. Nº 6A26748